



SEMICONDUCTOR DEVICE INCORPORATING INTERNAL POWER SUPPLY
FOR COMPENSATING FOR DEVIATION IN OPERATING CONDITION
AND FABRICATION PROCESS CONDITIONS

Ins
a/

a/

OColes
11/3/95

1 BACKGROUND OF THE INVENTION

The present invention relates generally to an improvement of performance of a semiconductor device and more particularly to a semiconductor device of high bit density realized in a structure suited for achieving high stability and enhanced reliability.

The technique for realizing the semiconductor devices in the form of integrated circuits having high bit density has made remarkable progress in recent years. Suppose, by way of example, a MOS dynamic random access memory (hereinafter referred to as ^a DRAM in abbreviation). The MOS DRAM of 1 Mbits is manufactured on ^a the mass production basis. A test chip of ^a 4-Mbit DRAM has already been reported. At the present state of the art, a 16-Mbit-DRAM is ^{undergoing} ~~en route~~ for development for practical applications. For realizing the semiconductor device of such high bit density, the size of the devices or elements constituting the semiconductor device as well as the size of wires must be made very small or fine in the range on the order of 0.5 μm to 1 μm . However, a great difficulty is encountered in fabricating such small (fine) devices or elements and wires accurately, giving rise to a problem that remarkable deviations can not be ^{avoided} ~~evaded~~. Taking the MOS DRAM as an example, the gate length and the threshold voltages which

1 mainly determine the characteristics of the MOS transistors
constituting the MOS DRAM will ^{vary} ~~very~~ significantly in
dependence on fluctuation in the device size and impurity
concentration. Considering the changes in the supply
5 voltage and the ambient temperature in the actual
operating condition, the access time of ^{the} ~~the~~ DRAM will vary
in the range from first to third order of magnitude.
Further, deviations due to the fabrication process
condition exert significant influence to the reliability
10 of the device. More specifically, degradation in the
dielectric breakdown strength (dioxide breakdown
strength) as well as degradation in the characteristics
(due to hot carriers) occur as the result of implementa-
tion of the elements in small or minute size. Further,
15 such characteristics concerning reliability of the
device depend by and large on the dispersion in the
implemented size.

As a hitherto known technique for improving
the stability and reliability of the characteristics
20 of the integrated semiconductor device, there is known
a method of operating the on-chip elements by lowering
the externally supplied voltage with the aid of an
on-chip voltage limiter provided on the semiconductor
device chip, as is disclosed in U.S. Patent No. 4,482,985.

25 However, in the prior known techniques
mentioned above, no consideration is paid to the
influence of the conditions in the fabrication process
condition and the operating condition to the electric

1 characteristics and reliability, and thus it has been
difficult to realize ^athe semiconductor device of high
stability and improved reliability.

Besides, because no consideration is made
5 concerning the influence of the condition in the
fabrication process, yield of the products of satis-
factory quality in the manufacturing on ^athe mass produc-
tion basis is low, giving rise to a problem that high
manufacturing cost is involved.

10 SUMMARY OF THE INVENTION

It is therefore an object of the present
invention to realize a semiconductor device enjoying
high stability and improved reliability by protecting
the electrical characteristics and the reliability
15 against changes, notwithstanding ^aof deviation or
variation in the condition of the fabrication process
condition and the operating condition.

In view of the ^{the}above and other objects which
will be more apparent as ^adescription proceeds, it is
20 proposed according to an aspect of the present
invention to control the operation voltage and/or
operation current of circuits incorporated in the semi-
conductor device in dependence on deviation or variation
in the fabrication process condition and the operating
25 condition.

^aAccording to ^{an embodiment}the teaching of the present
invention, the operation voltage and/or operation current

1 of the circuits and/or elements (devices) incorporated
in the semiconductor device is controlled in accordance
with the electrical characteristics ~~and reliability,~~
whereby ^a the semiconductor device of high stability
5 and enhanced reliability can be realized.

These and other objects and many of the
attendant advantages of the present invention will be
readily appreciated as the same becomes better under-
stood by reference to the following detailed description
10 when considered in connection with the accompanying
drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 to 6 are schematic diagrams for
illustrating the basic principle underlying the present
15 invention;

Figs. 7 to 52 are schematic circuit diagrams
showing exemplary embodiments of the invention; and
Figs. 53 to 70 are schematic circuit diagrams
showing exemplary embodiments of the invention applied
20 to DRAM (dynamic random access memory) and SRAM
(static random access memory).

^{Present Invention} ~~DESCRIPTION OF THE PREFERRED EMBODIMENTS~~

^{a Detailed} Fig. 1 is a schematic diagram for illustrating
the basic principle underlying an embodiment of the
25 present invention. In this figure, reference numeral 1
denotes a semiconductor chip, 2 denotes an internal

1 circuit inherent to a semiconductor device, and a
numeral 3 denotes a control circuit implemented
according to the invention for generating control
signals or controlled internal voltages in accordance
5 with ^adeviation in the condition in the fabrication
process as well as the operating condition in which
the semiconductor device is used. The control signal
or internal voltage as generated is utilized for
controlling operation of the internal circuit 2 by way
10 of a control bus or line 5. Although a single line 5
is shown, it will be readily understood that a number
of ~~the~~ signal lines may be prepared in the form of a
bus in conformance with the configuration of the internal
circuit 2.

15 According to the illustrated embodiment of
the invention, the characteristics of the internal
circuit 2 can be maintained in predetermined constant
relationship in conformance with the fabrication
process condition and the operating condition, whereby
20 ^a~~the~~ semiconductor device enjoying high stability and
improved reliability can be realized.

/ Fig. 2 shows another exemplary embodiment of
the present invention, which is so arranged that an
operation characteristic of the internal circuit 2 such
25 as, for example, operating speed, operating current or
the like is detected by a detecting or sensing line 6,
whereby a corresponding control signal is generated.
In this respect, the semiconductor device shown in

1 Fig. 2 differs from the one shown in Fig. 1.

In the case of the embodiment of the invention shown in Fig. 2, dynamic characteristics of the circuit 2 are detected straightforwardly for generating the control signal. Thus, the arrangement shown in Fig. 2 allows the control to be performed with a higher accuracy as compared with that of the device shown in Fig. 1, whereby ^athe semiconductor device can be realized which enjoys further improved stability and reliability. It goes without saying that a ^{plurality}~~number~~ of the sensing lines 6 may be provided, if necessary.

Fig. 3 shows a further embodiment of the invention which differs from the one shown in Fig. 2 in that a detecting or monitor circuit 4 having characteristics similar to those of the internal circuit 2 is provided for detecting the operation characteristics thereof.

With this arrangement, the operation characteristics of the internal circuit can be detected indirectly in terms of the characteristics of the detecting or monitor circuit 4 even in the case where no proper circuitry is provided for detecting the operation characteristics of the circuit 2, whereby the control can be so performed that the characteristics of the circuit 2 ^{bear}~~bears~~ a predetermined relation.

In the case of the semiconductor device shown in Fig. 3, the detecting circuit 4 is also under the control of the control circuit 3 which serves to

1 vary the characteristics of the detecting or monitor
circuit 4 ^{in a manner} similarly to the internal circuit 2. It
is conceivable to operate the ^{similar} ^{control of} detecting circuit 4
independent of the internal circuit 2 in accordance with
5 the envisaged applications of the semiconductor device.

Fig. 4 is a schematic diagram showing a
version of the embodiment illustrated in Fig. 1.

In the case of the semiconductor device shown in Fig.
4, a power supply source voltage is fed to the internal
10 circuit 2 from the control circuit 3 by way of a power
supply line 5I. The instant embodiment of the invention
is suited for the internal circuit implemented with
small or fine elements. More specifically, by setting
the potential on the power supply line 5I at a value
15 lower than the voltage which the elements constituting
the internal circuit 2 can withstand, the semiconductor
device constituted by the fine elements with high bit
density can be operated while maintaining ~~the~~ high
stability and reliability. Further, since there arises
20 no necessity to lower the external voltage, no burden
is imposed on the user. In the case of the dynamic
random access memory or DRAM, as the bit density is
increased from 256 K bits to 1 M bits and hence to 4 M
bits, the constituent elements have to be realized in
25 more and more fine (minute) structure. In that case,
lowering of the external voltage to cope with the
lowering of the voltage withstanding capability of the
constituent elements is undesirable, in order to assure

1 the compatibility with the conventional devices. For
this reason alone, the embodiment shown in Fig. 4 is
advantageous. Although a plurality of control lines
are shown in Fig. 4, the operation characteristics
5 of the internal circuit 2 can be stabilized by
controlling the voltage by means of the control circuit.
Further, the voltage control may be carried out such
that ^avariation in the internal voltage with reference
to the external voltage V_{CC} can be first compensated, ^{for}
10 being followed by compensation of variations in the
characteristics of the internal circuit 2 brought about
by changes in the environmental conditions such as
temperature and deviations in the fabrication process
condition. Needless to say, the control circuit to
15 which the external voltage V_{CC} is applied directly is
implemented by using the elements having the voltage
withstanding capability or the breakdown strength
exceeding the external voltage V_{CC} . ^{new} However, there may
exist some application in which a part of the control
20 circuit has to be constituted by ^afine element of lower
breakdown strength in an effort to enhance the bit density
or ^awith an attempt to make the characteristics of the
control circuit coincide with those of the internal
circuit. To this end, a voltage transformer circuit
25 3A may be provided internally in the control circuit 3,
whereby a voltage lower than the level V_{CC} is supplied
through an output line 5I to the internal circuit 2
as well as the circuitry 3B of the low breakdown strength

1 incorporated in the control circuit 3, as is shown in
Fig. 5. With this arrangement of the semiconductor
device, the integration or bit density thereof can be
further enhanced because the circuits inclusive of the
5 control circuit can be realized with fine (minute)
elements. Besides, since the control circuitry 3B and
the internal circuit 2 can be constituted by ~~the~~ elements
having identical characteristics, variation in the
operation characteristics of the internal circuit 2
10 can be controlled very precisely on the basis of
corresponding variations in the characteristics of the
control circuitry 3B, to a further advantage. ~~It~~ It should
however be mentioned in conjunction with the illustrative
embodiments shown in Figs. 4 and 5 that some of the
15 constituent elements thereof which exhibit a high
breakdown strength (voltage withstanding capability) may
be operated with the external voltage V_{CC} , as occasion
requires. Additionally, it goes without saying that
the semiconductor devices shown in Figs. 2 and 3 may
20 equally be realized with the fine elements having low
breakdown strength in the manner similar to the semi-
conductor devices shown in Figs. 4 and 5. ~~In~~ In the
exemplary embodiments of the invention as illustrated
in Figs. 1 to 5, it is assumed that ~~the~~ ^a single control
25 circuit is provided on one semiconductor chip. It
should however be appreciated that the internal circuit
2 may be divided into several ^{circuits} ~~circuitries~~ each being
provided with the respective control circuitry. To

a
a
1 this end, the arrangements shown in Figs. 1 to 5 may
of course be combined appropriately on ^athe case-by-
case basis. With the arrangement that the internal
circuit 2 is divided into several ^{circuits}~~circuitries~~ for
5 accomplishing the control of the operation character-
istics thereof, such control can be achieved for
realizing the optimum operation characteristics for the
individual functions of the divided circuitries.

a
Fig. 6 is a view illustrating ^{in graph form}~~graphically~~
10 such control that the operating speed of the circuit
is maintained constantly at values differing from one
another. More specifically, a broken curve C_{11} shown
in this figure represents the operation speed of a
conventional circuit incorporating no control circuitry.

15 As will be seen from this curve, the operating speed
varies significantly in dependence on the fabrication
process condition and the operating conditions. In
contrast, a circuit incorporating a number of control
^{circuits}~~circuitries~~ according to the teaching of the ^{present}~~invention~~
20 can exhibit a constant high speed as indicated by

a
a solid line curve B_{11} . Of course, the circuit
incorporating the control circuitries and destined
for low-speed operation can be maintained at a desired
constant low speed, as indicated by a solid line curve
25 A_{12} . [#]In the case of an output circuit or the like, by
way of example, when charge and discharge of the output
load capacitance is performed at a high speed, noise
is likely to be generated in the power supply source

1 to exert adverse influence to the operation of the
internal circuits or semiconductor devices disposed
in the vicinity. In that case, by controlling only
the output circuit so that it operates at a low speed,
5 the operating speed can be maintained at a constant
value without lowering the speed of the whole circuit
system. Although such control that the circuit
operation is maintained independent of the fabrication
process condition and the operating condition is
10 described, this is only ^{one} ~~by way of~~ example. The circuit
operation speed may be imparted with a desired dependency
on a desired factor, as occasion requires. For example,
such control can be equally realized that the operating
speed of a circuit is increased as a function of
15 ^{increases} ~~increasing~~ in the temperature. In that case, control
may be made such that a delay involved due to resistance
of wiring conductors within a semiconductor device or
wiring conductors interconnecting the semiconductor
devices can be compensated for by the increased operating
20 speed brought about by a temperature rise, to thereby
maintain constant the speed of the semiconductor device
or that of the whole system including the semiconductor
devices. # As will now be appreciated, according to the
^{embodiments} ~~present~~ ~~teachings of the invention incarnated in the embodiments~~
25 shown in Figs. 1 to 6, ~~the~~ circuit characteristics can
be protected against variation brought about in the
fabrication process, which in turn means that yield
of the products of satisfactory quality fabricated on

1 the mass production basis can be improved. Further,
since the circuit characteristics can be ^{protected} ~~prevented~~
from variations as caused by changes in the operating
condition, reliability of a system such as a computer
5 which is realized by using the semiconductor devices
according to the invention can be improved significantly.
There exist certain applications where synchronization
is required between operations of the two ^{circuits} ~~circuitries~~
incorporated in the circuit 2. In that case, by
10 adopting the inventive circuit arrangement, the timing
margin can be set at a minimum value by virtue of the
invariability of the characteristics. This in turn
means that the operating speed of the semiconductor
device can be correspondingly increased. In the case
15 of DRAM (dynamic random access memory), for example,
synchronization has to be established between the
memory cell array and peripheral circuitries. In that
case, by adopting the teachings of the present
invention, the timing margin can be set to a minimum,
20 whereby operating speed of the DRAM can be increased.
The same
The same holds true in the case where synchronization in
operation must be established among more than two
semiconductor devices. In other words, operating speed
of a system such as a computer constituted by a number
25 of semiconductor devices can be increased by applying
^{present invention} ~~the inventive teachings~~ to these semiconductor devices.
In the embodiments shown in Figs. 4 and 5, a so-called
TTL interface with the positive power source of V_{CC} is

1 assumed to be employed. It should however be appreciated
that essentially ^{the} same effects can be attained even when ^{an}
ECL interface is employed. The following description
will be made on the assumption that the TTL interface
5 is employed. However, this never means that the
invention is restricted to the use of TTL interface.
The present invention can be equally realized by using
the ECL interface.

In the following, exemplary embodiments of
10 the present invention will be described with reference
to more concrete circuit configurations. In the first
place, description is directed to a method of controlling
the characteristics of a driver circuit constituting
a basic circuitry of an integrated circuit device.
15 ^{7A} / Fig. ⁷ shows ^{a detailed embodiment} ~~one of the concrete embodiments~~
of the present invention which is designed for controlling
a driver circuitry incorporated in a circuit 2. In
the case of this illustrative embodiment, the charac-
teristics of the driver circuitry are controlled by
20 varying the power ^{7A} supply voltage of the circuit.

Referring to Fig. ^{7A} 7, an elementary circuitry 2'
constituting a part of the circuit 2 is a CMOS ^{inverter} ~~inverter~~
composed of a P-channel MOS transistor T_{p1} and an N-
channel MOS transistor T_{n1} . It should however be
25 understood that the elementary circuitry 2' may be
^{another} ~~other~~ logic circuit such as ^a NAND and ^{a circuit} ~~NOR~~ ^{circuitries}.

Further, it may be composed of bipolar transistors or
a combination of a bipolar transistor and a MOS transistor,

a 1 or a circuit constituted by ^{a combination} ~~one of given combinations~~ of these circuit elements.

According to the instant embodiment of the invention, characteristics of the driver circuitry 2' and hence that of the whole circuit 2 can be controlled by varying a voltage V_{CONT} supplied from the control circuit 3 by way of the line 5, whereby a semiconductor device enjoying a high stability and an improved reliability can be realized. Value of the control voltage V_{CONT} is determined in dependence on the circuit configuration of the driver circuitries 2' to be controlled, as is ~~graphically~~ illustrated in Fig. 7B, by way of example. In order to maintain constant the operating speed of the CMOS ^{inverter} ~~inverter~~ while enhancing the reliability, the control voltage V_{CONT} may be varied in such a manner as illustrated in Fig. 7B in consideration of various factors. More specifically, the CMOS inverter exhibits a delay time t_d which bears a certain relation to a gate length L_g , a threshold voltage V_T , a thickness t_{ox} of gate oxide film, a channel conductance β_o , temperature T (absolute temperature) and a load capacity C_L , which relation is approximately given by

a 15 20

$$t_d \propto C_L \times \frac{1}{\beta_o} \times L_g \times \frac{1}{(V_{CONT} - V_T)} \times T^{1.5} \quad \dots\dots (1)$$

a In the actual circuits, the delay time may ^{deviate} ~~be deviated~~ more or less from the value determined by the above

25

1 expression for various reasons. It is however safe to
say that the relation given by the expression (1) ^{is} can
apply essentially valid ^{for} to the CMOS circuits in general.
Accordingly, the control voltage V_{CONT} may be varied
5 according to the relation given by the above expression
(1) so that the delay time t_d can be maintained constant.
^{There} ~~in more concrete~~, there exists such qualitative trend
that the delay time t_d can be held substantially constant
by increasing the value of the control voltage V_{CONT}
10 as the values of various variable factors (in the
case of channel conductance β_o , ^{the} reciprocal thereof)
are increased. In this way, the operating speed can
be maintained constant independent of variations in
the fabrication process condition and the operating
15 condition. In the case of the instant embodiment,
response to the change in temperature is also taken
into consideration. Consequently, performance of the
circuit can be maintained substantially constant
regardless of ^a variation in the ambient temperature as
20 well as such variation in temperature as caused by
^{differences} ~~difference~~ in the amount of heat generated by the
semiconductor device ^{when in} ~~between~~ the standby state and ^{when in} the
ordinary operating state ~~thereof~~, by way of example.

In connection with the above-mentioned
25 expression (1), it is assumed that the values of
factors L_g , V_T , t_{ox} and β_o are ^{the} same in both P-channel
MOS transistor and N-channel MOS transistor. However,
in actuality, these values differ from one to another

a
1 element. However, in both P- and N-MOS transistors,
difference is found only in respect to the polarities
of voltage and current. Except for this difference,
the relation given by the expression (1) ^{is} ~~can apply~~ valid
5 without need for any further modification. Accordingly,
both MOS transistors are handled without discrimination
except for the case where such discrimination is
necessary.

As described hereinbefore, it is also
10 contemplated by the invention to establish a desired
dependence relation between the circuit speed and
desired parameter(s) in place of the control for
maintaining the operating speed of the circuit to be
constant. By way of example, when it is desired to
15 increase the operating speed of the circuit as a
function of temperature rise, control may be made from
the expression (1) in accordance with

$$(V_{\text{CONT}} - V_T) \propto T^{-n} \text{ instead of } (V_{\text{CONT}} - V_T) \propto T^{-1.5}$$

where n is selected greater than 1.5.

Next, breakdown voltage will be considered.

a
20 The dioxide breakdown voltage (dielectric breakdown
strength) becomes ^{lower} ~~lowered~~ as the gate length L_g and
thickness t_{ox} of the gate oxide film are decreased.
In this connection, the control voltage V_{CONT} may also
be controlled in the manner illustrated in Fig. 7B.
25 Further, because of the phenomenon discovered recently

1 that the carriers of high energy generated in the
vicinity of the drain domain of a MOS transistor are
injected into the gate oxide film to thereby cause
the threshold voltage to be increased, involving
5 degradation of the characteristics such as lowering
of the channel conductance, the breakdown voltage
(referred to as the hot carrier breakdown voltage)
defining the upper limit of the operation voltage
becomes lower as the gate length L_g and the gate oxide
10 film thickness t_{ox} become smaller with the temperature
T being lower. To deal with this phenomenon, the voltage
 V_{CONT} may be controlled in such a manner as illustrated
in Fig. 7B. By virtue of such control, the problem of
degradation of the characteristics can be ^{avoided} ~~evaded~~, even
15 when the hot carrier breakdown strength is lowered due
to deviations ascribable to the ^{fabrication} ~~fabrication~~ process
condition. Besides, even when the threshold voltage
is increased and/or when the channel conductance is
decreased because of occurrence of the above-mentioned
20 hot carrier phenomenon and other factors after operation
for an extended period, the circuit characteristics can
be maintained substantially constant through the control
illustrated in Fig. 7B.

As pointed out hereinbefore, the embodiment
25 shown in Fig. ^{7A} ~~7A~~ is not restricted to the use of the
CMOS ^{inverter} ~~inverter~~ as the circuitry 2', but various other
^{circuits} ~~circuitries~~ can be employed. By way of example, a
BiCMOS ^{inverter} ~~inverter~~ shown in Fig. 8 may be employed. In

1 that case, a higher speed can be realized because the
output drive stage is constituted by the bipolar
transistors. In the circuit configuration shown in
Fig. 8, the collector of the bipolar transistor Q_{N3}
5 is connected to the external supply voltage V_{CC} . With
this arrangement, a major proportion of the output
current is ~~catered for from~~ ^{supplied by} the external power supply
source V_{CC} , whereby the driving capability of the
control circuit 3 can be decreased with the circuit
10 design being correspondingly simplified. Parenthetically,
in case the voltage withstanding capability of the
bipolar transistor is low, the driving capability of
the control circuit can be increased, wherein the
control voltage V_{CONT} is then applied to the collector
15 of the bipolar transistor Q_{N3} . ~~As the circuitry 2~~
~~shown in Fig. 6, circuits shown in Figs. 9 and 10,~~
respectively, may be employed.

Fig. 9 shows a circuit arrangement in which
the circuit shown in Fig. 7 is added with an output
20 buffer circuit constituted by MOS transistors T_{N3} and
 T_{N4} . The operation speed and the output voltage of
the circuit shown in Fig. 9 are controlled by the
control voltage V_{CONT} as with the case of the circuit
shown in Fig. 7 and is advantageous in that the driving
25 capability of the control circuit 3 can be made smaller
with the design being facilitated, as with the case
of the circuit shown in Fig. 8, because the drive
current for a load capacity connected to the output is

1 supplied from the external supply source V_{CC} .

Fig. 10 shows a circuit arrangement which differs from the one shown in Fig. 9 in that the N-channel MOS transistor T_{N3} in the latter circuit is
5 replaced by the bipolar transistor Q_{N3} . Because of higher driving capability of the bipolar transistor Q_{N3} , the load can be driven at a higher speed, while the driving capability of the control circuit 3 (Fig. 7A) can be made smaller.

10 In the case of the embodiments shown in Figs. 8 to 10, the circuit characteristics can be controlled with the aid of the control voltage V_{CONT} in the manner similar to that of the circuit shown in Fig. 7.

15 Fig. 11A shows another embodiment of the invention ~~destined~~ for controlling the characteristics of the driving circuit. This figure shows only the circuit portion corresponding to the elementary circuitry 2' shown in Fig. 7. A P-channel MOS transistor
20 T_{P2} and an N-channel MOS transistor T_{N2} are inserted between the CMOS ^{inverter} ~~inverter~~ constituted by P- and N-channel MOS transistors T_{P1} and T_{N1} and the external supply voltage V_{CC} on one hand and the ground on the other hand, respectively, wherein the gate voltages
25 V_{CONT} and V'_{CONT} of the MOS transistors T_{P2} and T_{N2} are controlled to thereby control the operation current of the CMOS ^{inverter} ~~inverter~~ so that the operation speed is controlled. More specifically, the operation speed is

a
1 increased as ^athe current is increased and vice versa.
The delay time t_d exhibits the tendency similar to that
given by the expression (1) for various variable
factors. Accordingly, the gate control voltage V_{CONT}
5 for the P-channel MOS transistor T_{P2} is varied from a
large value to a small value while the gate control
voltage V_{CONT}' for the N-channel MOS transistor T_{N2}
is varied from a small value to a large value, as the
factors L_g , V_T , t_{ox} , $1/\beta_o$, T and C_L are increased,
10 whereby the delay time t_d can be maintained to be
substantially constant.

In the instant embodiment, the operation
current is supplied directly from the power supply
source, wherein the control voltages V_{CONT} and V_{CONT}'
15 can drive only the gates of the MOS transistors T_{P2}
and T_{N2} , respectively. Thus, the driving capability
of the control circuit 3 can be made smaller, which
in turn means that the circuit design can be extremely
facilitated. Although the control is performed with
20 both channel MOS transistors T_{P2} and T_{N2} in the instant
embodiment, it falls within the purview of the
invention to provide only one of these MOS transistors
in dependence on the envisaged application. In
conjunction with the embodiment shown in Fig. 1, it
25 is to be added that when the ON-resistances (resistance
in the conducting state) of the MOS transistors T_{P1} and
 T_{N1} are realized greater than those of the transistors
 T_{P2} and T_{N2} by increasing the gate widths of the MOS

a

a
1 transistors T_{P1} and T_{N1} when compared with those of the
transistors T_{P2} and T_{N2} , the output current can be
determined by the ON-resistances of the MOS transistors
 T_{P2} and T_{N2} , whereby the speed control can be ^{greatly} ~~much~~
5 facilitated.

a
a
a
In the embodiment shown in Fig. 11, a MOS
^{inverter} ~~inverter~~ is employed. It should however be understood
that the invention is not restricted to ^a ~~the~~ MOS ^{inverter} ~~inverter~~
but can equally be applied to various types of logic
10 circuits such ^{as} a NAND circuit, NOR circuit or the like.
To this end, the circuit portion denoted by DRIV may
be replaced by a logic circuit imparted with the driving
function.

a
15 Figs. 12A and 12B show further embodiments of
the present invention in which the control principle
described ⁱⁿ ~~by~~ reference to Fig. 11 is applied to a
BiCMOS drive circuit which has a higher driving
capability as compared with the CMOS circuit. As is
well known in the art, in the BiCMOS circuit, the base
20 current is fed to the base of a bipolar transistor from
a MOS transistor to be amplified by the bipolar transistor
for driving a load capacitance. Accordingly, the circuit
operation speed can be controlled by controlling the
base current with the circuit of such configuration as
25 shown in Fig. 12A. Referring to this figure, when the
input IN assumes a low level, P-channel transistor
 T_{P2} and N-channel MOS transistor T_{N3} are turned on,
being followed by turn-off of N-channel MOS transistors

1 T_{N4} and T_{N1} . As the result, the bipolar transistor
 Q_{N3} is turned on with the transistor Q_{N4} being turned
off. In this state, the base current flowing through
the bipolar transistor Q_{N3} can be controlled by the
5 P-channel MOS transistor T_{P2} having the gate supplied
with the control voltage V_{CONT} . Thus, the operation
speed can be controlled with the aid of the control
voltage V_{CONT} when the output is charged. On the
other hand, when the input IN assume a high level, the
10 bipolar transistor Q_{N3} is turned off with the transistor
 Q_{N4} being also turned on, whereupon discharge of the
output is initiated. At that time, the base current
of the bipolar transistor Q_{N4} is supplied from the
output OUT. This base current can be controlled by the
15 control voltage V_{CONT}' , which in turn means that the
discharge rate of the output can be controlled by the
control voltage V_{CONT}' . In this manner, the operation
speed of the BiCMOS drive circuit according to the
instant embodiment can be controlled. In conjunction
20 with the above-mentioned operation speed control of
the BiCMOS drive circuit, it should be mentioned that
the circuit portion DRIV shown in Fig. 11 may be simply
replaced by a BiCMOS circuit shown in Fig. 12B. In
that case, the current is determined by the MOS
25 transistors T_{P2} and T_{N2} shown in Fig. 11A. Consequently,
more accurate control can be accomplished when compared
with the control only of the base current as with the
case of the BiCMOS circuit shown in Fig. 12A. Further,

1 since the capacity of the MOS transistors constituting
the circuit portion DRIV can be reduced by the driving
capability of the bipolar transistors, there can be
achieved an advantage that the input capacity as
5 observed from the side of input IN is small. In
other words, high operation speed can be realized
because the load in the preceding stage is reduced.

The method of controlling the current by
inserting the MOS transistor between the power supply
10 source and the driving circuit DRIV, as is shown in
Fig. 11, can find other applications. Fig. 13 shows
another embodiment of the invention which is applied
to a level conversion circuit for deriving a large
output amplitude from an input amplitude. Operation
15 of the level conversion circuit will be described by
reference to Fig. 14. When the input IN assumes a
high level V_A in the state where a high potential is
applied to the gate E, potential at a circuit point F
assumes a value represented by $(V_A - V_T)$ by way of
20 the N-channel MOS transistor T_{N3} . Subsequently, when
the potential at E becomes low, the P-channel MOS
transistor T_{P1} is turned off with the N-channel MOS
transistor T_{N1} being on, whereupon the output OUT
assumes a level of zero volt. When the potential at
25 F rises up to a level V_H , potentials at A and C are at
a level V_A with the MOS transistor T_{N3} being off.
Accordingly, the potential at the circuit point F is
protected against being lowered due to the current flow

1 from the circuit point F toward IN. On the other hand,
when the input IN assumes a low potential level in the
state in which E is at a high potential, the MOS
transistor T_{N3} is turned on, resulting in that the
5 circuit point F assumes the same low potential level
as that at IN. As the consequence, the MOS transistor
 T_{P1} is turned on with T_{N1} being turned off, whereby
the output OUT is charged to the high level V_H . In
connection with this circuit, it is noted that when a
10 period t_{CE} intervening between the time point at which
IN assumes the high level V_A and the time point at
which the potential at E become low is long, as
indicated by a broken line in Fig. 14, the potential
at the circuit point F remains at $V_A - V_T$ for a time
15 being. Then, there may arise such a situation in which
a penetration current flows through the MOS transistors
 T_{P1} and T_{N1} , respectively, giving rise to occurrence
of a period during which the output OUT remains at
an inadequately low potential level. For this reason,
20 it is desirable to shorten the duration of the period
 t_{CE} . This can be achieved by changing over the
potential at E to low potential level simultaneously
when the input IN assumes the high level. In this way,
the problem mentioned above can be solved.

25 As will now be appreciated, in the case of
the circuit arrangement shown in Fig. 13, the amplitude
 V_A of the input IN can be transformed to a large
amplitude V_H . At that time, since the current can be

1 controlled by the MOS transistors T_{P2} and T_{N2} , the
circuit can be operated at a desired constant speed.
The circuit configuration shown in Fig. 13 can be
effectively and advantageously utilized as a circuit
5 for deriving a high output voltage from an input
voltage, as exemplified by a word driver circuit for
a dynamic memory.

Fig. 15 shows another embodiment of the
invention for controlling the operation speed of a driver
10 circuit. In this circuit, the inverter is so implemented
as to receive directly the output from the current
control MOS transistor in the circuit shown in Fig. 11.
Referring to Fig. 15, when the input voltage assumes
a high level, the P-channel MOS transistors T_{P1} and T_{P3}
15 are turned off with N-channel MOS transistors T_{N1} and
 T_{N3} being turned on. As the result, the control
voltage V_{CONT} is applied to the gate of the P-channel
MOS transistor T_{P2} , while the potential at the gate of
the N-channel MOS transistor T_{N2} assumes zero volt.
20 As a consequence, the gate of the P-channel MOS
transistor T_{P2} is supplied with the control voltage
 V_{CONT} , while the gate potential of the N-channel MOS
transistor T_{N2} becomes zero volt. Accordingly, the
P-channel transistor T_{P2} is turned on with the N-
25 channel transistor T_{N2} being turned off, whereby a
current controlled to a desired value by the control
voltage V_{CONT} is obtained at the output to charge a
load. In contrast, when the level of the input IN

1 becomes low, the P-channel MOS transistor T_{P2} is turned
off while the N-channel MOS transistor T_{N2} is turned
on to thereby initiate the discharge operation,
whereupon the output OUT assumes zero volt level.
5 Since the voltage V_{CONT} is applied to the gate of the
N-channel MOS transistor T_{N2} at this time point, the
rate of discharge can also be controlled. The embodiment
shown in Fig. 15 is very suited for the high-speed
operation because of absence of serial connection of
10 two MOS transistors between the power supply source
and the output OUT. Further, the control can be much
facilitated when compared with the circuit shown in
Fig. 11 where influences of variation in the charac-
teristics of two serially connected transistors has to
15 be taken into consideration.

In the foregoing, various methods of controlling
the operation speed of the driver circuit have been
explained. In this conjunction, it will be noted that
the external voltage V_{CC} is utilized in the circuits
20 shown in Figs. 12 to 15. Under the circumstances, there
may possibly arise such problem that difficulty is
encountered in compensating for the variation in the
external voltage V_{CC} . To cope with this problem, it
is possible to incorporate the voltage conversion or
25 transformer circuit 3A in the control circuit 3, as
shown in Fig. 5, for thereby maintaining the output
voltage V_I to be constant, in order to realize the
stabilized operation of the internal circuit notwithstanding

1 of variation in the external voltage V_{CC} . In this
case, when the internal voltage V_I is set at low
level, the small or fine elements having low voltage
withstanding capability or breakdown strength can be
5 operated stably. Fig. 16 shows another exemplary
embodiment of the invention in which the voltage
transformer circuit mentioned above is provided on
chip. In Fig. 16, a reference symbol 5I denotes a
power supply line for supplying a voltage V_I to the
10 internal circuit 2 and a circuitry 3B incorporated in
the control circuit from the voltage transformer
circuit 3A. Further, a reference symbol ICL denotes
current control circuitries for controlling the current
to the individual circuitries DRIV such as MOS transistors
15 T_{P2} , T_{N2} shown in Fig. 11. With this circuit arrange-
ment, the fine elements of small size can be operated
stably with the constant voltage V_I independent of
the external voltage V_{CC} at desired speeds corresponding
to the functions of the individual circuitries.

20 Fig. 17 shows a further embodiment of the
present invention adapted to control the operation speed
of a CMOS inverter. According to this embodiment,
voltages of substrates SBP1 and SBP2 of P-channel MOS
transistor T_{P1} and N-channel MOS transistor T_{N1} are
25 controlled to thereby control the threshold voltages
of these transistors T_{P1} and T_{N1} for controlling
ultimately the operation characteristics of the inverter.
The instant embodiment is advantageously suited to

1 compensate for variation in the characteristics brought
about by fluctuation of the threshold voltage.

Although the embodiment shown in Fig. 17
is intended for application to the CMOS inverter, it
5 should be noted that the instant embodiment can be
equally applied to other circuits such as BiCMOS
inverter in which MOS transistors are employed. Besides,
it is to be added that the control of the substrate
voltages may be combined with the other control methods
10 described hereinbefore.

The foregoing description made by reference
to Figs. 7 to 17 is primarily directed to the methods
of controlling the characteristics of the driver
circuits such as invertors, non-invertor NAND circuits
15 and others. It is however noted that a differential
amplifier in the form of integrated circuit for producing
an output in dependence on difference between input
voltage is also used widely. The following description
will be made on the embodiments of the invention applied
20 to the differential amplifiers.

Fig. 18 shows an embodiment of the invention
in which the control method described hereinbefore
by reference to Fig. 11 is applied to the control of
operation speed of a differential amplifier constituted
25 by MOS transistors. In Fig. 18, reference symbols IN1
and IN2 denote differential input terminals, and OUT1
and OUT2 denote differential output terminals. In the
case of this differential amplifier, the operation speed

1 varies in dependence on deviations in the fabrication
process condition as well as variations in the
operating condition in a manner similar to the case
of the device shown in Fig. 11A. Accordingly, by
5 varying the control voltages V_{CONT} and V_{CONT}' in the
similar manner as illustrated in Fig. 11B to thereby
vary the operation current correspondingly, it is
possible to control the operation speed with the
fabrication process condition and the operating condition
10 being taken into account. The output voltage of this
differential amplifier is determined by a product of
the operation current and ON-resistances (i.e.
resistance in the conducting state) of the load MOS
transistors T_{PL} and T_{PL}' . Accordingly, by controlling
15 the control voltages V_{CONT} and V_{CONT}' so that the
ratio between the ON-resistance of the MOS transistor
 T_{NC} which determines the operation current and the
ON-resistance of the load MOS transistors T_{PL} and T_{PL}'
is constant, the operation speed can be controlled
20 while holding constant the output voltage, i.e. the
product of the operation current and the ON-resistances
of the transistors T_{PL} and T_{PL}' .

Fig. 19 shows another embodiment of the
invention which differs from that shown in Fig. 18 in
25 that the MOS transistors T_{NA} and T_{NA}' shown in Fig. 18
are replaced by NPN-bipolar transistors Q_{NA} and Q_{NA}' ,
respectively. With the circuit configuration shown
in Fig. 19, substantially same effects as those of the

1 circuit shown in Fig. 18 can be achieved. Moreover,
the amplification factor can be increased.

Fig. 20 shows a version of the embodiment
shown in Fig. 19. In the embodiment shown in Fig. 20,
5 the current control transistor T_{NC} shown in Fig. 19 is
replaced by an NPN-bipolar transistor Q_{NC} and a resistor
 R_C . With the circuit configuration shown in Fig. 20,
the operation speed can be controlled as with the
case of the embodiments shown in Figs. 18 and 19.
10 Furthermore, the amplification factor can be increased
because the operation current is made to be more
constant.

In case application of the external voltage
 V_{CC} presents a problem in respect to the dielectric
15 breakdown strength or variation in the characteristics
brought about by fluctuation in the voltage V_{CC} , a
desired voltage can be derived by providing the voltage
limiter or transformer circuit 3A on chip, as in the
case of the embodiment shown in Fig. 5.

20 In the foregoing, various preferred embodiments
for controlling the elementary circuitries constituting
the internal circuit 2 (Figs. 1 to 5) have been described.
Next, description will be turned to exemplary embodi-
ments of the control circuit 3.

25 Fig. 21 shows a concrete example of the
control circuit 3. In this figure, a reference symbol
 T_{PR} denotes a P-channel MOS transistor and CC denotes
a constant current power source for supplying a constant

1 current i . According to this embodiment, a gate
voltage required for causing a constant current to
flow through the P-channel MOS transistor T_{PR} is
constantly outputted regardless of deviation in the
5 fabrication process condition, i.e. deviation in the
gate length, threshold voltage, gate oxide film thick-
ness and other factor as well as variation in the
operating condition. Accordingly, this embodiment
is advantageously suited for use as the control voltage
10 (V_{CONT}) generating circuit to be used in combination
with the circuits described hereinbefore by reference
to Figs. 11 to 13, Fig. 15 and Figs. 18 to 20, respec-
tively. The P-channel MOS transistor T_{PR} shown in
Fig. 21 is connected to the transistor T_{P2} shown in
15 Figs. 11 to 13, and Fig. 15 or the transistors T_{PL} and
 T_{PL}' shown in Figs. 18 to 20 in the form of a current
mirror connection well known in the art. Accordingly,
by selecting appropriately the size of the transistor
 T_{P2} or T_{PL} and T_{PL}' relative to that of the transistor
20 T_{PR} , the operation current in the concerned circuits
can be controlled to a given constant value.

Fig. 22 shows another embodiment of the
control circuit (3) which differs from the one shown
in Fig. 21 in that an N-channel MOS transistor is
25 employed. The control circuit shown in Fig. 22 is
optimal for use as the control voltage (V_{CONT}') generating
circuit in combination with the circuits shown in Figs.
11 to 13, Fig. 15 and Figs. 18 and 19, respectively.

1 With this circuit shown in Fig. 22, substantially
same effects as those of the circuit shown in Fig. 21
can be achieved.

Fig. 23 shows another embodiment of the
5 invention which corresponds to a combination of the
circuits shown in Figs. 21 and 22. With this circuit
arrangement, the control voltages V_{CONT} and V_{CONT}'
for the circuits shown in Figs. 11 to 13, Fig. 15 and
Figs. 18 and 19, respectively, can be generated
10 simultaneously. Additionally, since these control
voltages V_{CONT} and V_{CONT}' are generated on the basis of
one and the same constant current power supply source,
there can be obtained the control voltages (V_{CONT} and
 V_{CONT}') of extremely high stability and mutual
15 matchability.

Fig. 24 shows still another concrete example
of the control circuit (3) which is realized by a
serial connection of a P-channel MOS transistor T_{PR}
and an N-channel MOS transistor T_{NR} for generating the
20 control voltage V_{CONT} . With this circuit configuration,
the value of the control voltage V_{CONT} undergoes
influence of deviations in the process conditions in
fabrication of the P- and N-channel MOS transistors
as well as variations in the operating conditions.
25 Accordingly, this circuit can be advantageously used
as the V_{CONT} -generating circuit in the devices shown
in Figs. 7 to 10, respectively.

Fig. 25 shows another embodiment of the

1 control circuit (3) according to the invention which
differs from that shown in Fig. 24 in that an
amplification circuit composed of an amplifier 7 and
a feedback circuit having a feedback ratio β is
5 additionally provided on the output side. By selecting
a sufficiently large value for the amplification
factor, the output control voltage V_{CONT} is given by

$$V_{\text{CONT}} = \frac{V_0}{\beta}$$

Thus, by setting the feedback ratio β at an appropriate
value, the control output voltage V_{CONT} of a desired
10 value can be obtained. Accordingly, in addition to
reflecting the influence of deviation in the fabrication
process condition as well as variation in the operating
condition to the value of the voltage V_0 , it is also
possible to take into account the dependency of the
15 fabrication process condition and the operating
condition in determining the feedback ratio β . In other
words, the influence of deviation in the fabrication
process condition and variation in the operating
condition to the control voltage V_{CONT} can be properly
20 taken into consideration by selecting appropriately the
feedback ratio β .

Fig. 26 shows a concrete example of the
constant current power source CC. As will be seen in
this figure, the constant current power source CC_1 is
25 constituted by resistors R_1 to R_4 and an NPN-bipolar

1 transistors Q_{N1} and Q_{N2} . According to this embodiment
of the present invention, the base voltage B_{N1} of
the bipolar transistor Q_{N1} assumes a constant value
given by $V_{BE}(R_2 + R_3)/R_3$, provided that the current
5 amplification factor of the bipolar transistor is
sufficiently large. In the above expression, V_{BE}
represents a forward voltage between emitter and base
of the bipolar transistor.

Accordingly, a constant current i given by
10 the following expression can flow.

$$i = \left[\left(V_{BE} \frac{R_2 + R_3}{R_3} \right) - V_{BE} \right] / R_4$$

$$= V_{BE} \frac{R_2}{R_3 \times R_4} \quad \dots\dots (2)$$

Since the base-emitter voltage V_{BE} is substantially
insusceptible to the deviation in the fabrication
process condition, there can be outputted a stable
current.

15 Since the current i flows toward the ground
from the external source, this embodiment is advantage-
ously suited for use as the constant current power
source in such circuit as shown in Fig. 21.

Fig. 27 shows another exemplary embodiment
20 of the constant current power source which is realized
by using PNP-bipolar transistors Q_{P1} and Q_{P2} .
Operation of this constant current circuit is utterly

1 same as that of the circuit shown in Fig. 26 with only
difference in the polarity of voltage and current.

Because of the circuit configuration in which the
current i flows out from the voltage source V_{CC} , this
5 circuit is very suitable for the constant current
source in the circuit such as shown in Fig. 25.

Fig. 28 shows still another embodiment of
the constant current source of the type in which the
current flows out from a voltage supply source as in
10 the case of the circuit shown in Fig. 27. The constant
current source shown in Fig. 28 is however realized by
using NPN-bipolar transistors Q_{N1} and Q_{N2} . In the
case of this embodiment, there is a problem that the
operation current flowing through the resistors R_1 ,
15 R_2 and R_3 and the NPN-bipolar transistor Q_{N2} is added
to the constant current. However, influence of the
above-mentioned operation current may be neglected by
setting the current amplification factor of the
transistor Q_{N1} at a sufficiently large value.

20 According to the teaching of the invention
embodied in the circuit shown in Fig. 29, the constant
current supply source of the type in which the current
flows out from the voltage supply source V_{CC} can be
fabricated in a facilitated manner by using NPN-bipolar
25 transistors of high performance. Parenthetically, the
constant current supply source shown in Fig. 29 can
be used either in an arrangement in which the current
flows into the current source circuit or in an arrangement

1 in which the current flows out from the current source circuit.

By taking advantages of this feature, Fig. 29 shows an application of the above-mentioned constant
5 current supply source to the circuit shown in Fig. 23. With the circuit configuration shown in Fig. 29, the control voltages V_{CONT} and V_{CONT}' can be outputted simultaneously.

Fig. 30 shows a further embodiment of the
10 constant current supply source of the type in which the current flows out from the voltage supply source V_{CC} and which is realized by a current mirror circuit constituted by a current source CC implemented such that the current flows to the ground as in the case of the
15 constant current source shown in Fig. 26 and P-channel MOS transistors T_{PM} and T_{PM}' . By realizing the transistors T_{PM} and T_{PM}' in a same size, a current having a same value as the output current i of the current source CC can be derived externally from the
20 voltage supply source. By inputting this current to the N-channel transistor T_{NR} as in the case of the circuit shown in Fig. 22, the control voltage V_{CONT}' can be obtained. According to the instant embodiment, the output can be determined rather arbitrarily for
25 the current value of the current source CC by selecting appropriately the ratio in size between the P-channel MOS transistors T_{PM} and T_{PM}' .

Fig. 31 shows a modification of the constant

1 current supply source shown in Fig. 30. According to
the instant embodiment shown in Fig. 30, the voltage
generated through cooperation of the P-channel
MOS transistor T_{PM} and the current source CC is utilized
5 as the control voltage V_{CONT} . With this arrangement,
both control voltages V_{CONT} and V_{CONT}' can be generated
simultaneously, wherein the characteristics of both
voltages can be controlled with an improved matchability,
to further advantage.

10 Fig. 32 shows another embodiment of the
constant current supply source having a high stability
and realized by using MOS transistors.

In this figure, T_{N61} to T_{N63} designate N-
channel MOS transistors, respectively, wherein the MOS
15 transistor T_{N61} has a negative threshold voltage while
the transistor T_{N62} has a positive threshold voltage.
The threshold voltage of the MOS transistor T_{N63} may
be positive or negative. Symbols R_{61} to R_{63} designates
resistors, and 7 denotes a differential amplifier.

20 By setting the resistors R_{61} and R_{62} at a
same value while realizing the transistors T_{N61} and
 T_{N62} in the same size, the currents flowing to the
transistors T_{N61} and T_{N62} become equal to each other.
Consequently, the gate voltage V_{I6} of the transistor
25 T_{N62} has a value equal to difference between the
threshold voltages of the transistors T_{N61} and T_{N62} .
In this connection, it should be noted that the value
of difference between these threshold voltages is held

1 substantially constant independent of the fabrication
process condition and the operating condition.

In the circuit described above, the drain
current and the source current of the N-channel MOS
5 transistor T_{N63} is equal to each other. Accordingly,
the output current i is given by

$$i = \frac{V_{I6}}{R_{63}} \quad \dots\dots (3)$$

Thus, the output current having the same characteristics
as the gate voltage V_{I6} can be obtained, wherein the
value of the output current can be controlled arbitrarily
10 with the aid of the resistor R_{63} .

The constant current supply source according
to the instant embodiment can be used as the current
supply source CC in the circuit shown in Fig. 31 as
well as other circuit to make possible the character-
15 istic control with high stability.

Further, according to the above-mentioned
embodiment, the circuit can be implemented even without
resorting to the use of the bipolar transistors and
thus is suited for the integrated circuit constituted
20 by using MOS transistors.

Fig. 33 shows a further embodiment of the
constant current supply source advantageously suited
to the use for the circuits shown in Figs. 21 to 25
and Figs. 30 and 31. According to this embodiment, a
25 current generator known per se is made use of as the

1 constant current supply source which can supply a
 current which is highly stabilized against fluctuations
 in the source voltage and the ambient temperature
 among others.

5 Referring to Fig. 33, reference symbols Q_{51}
 to Q_{56} designate bipolar transistors and R_{51} to R_{55}
 designate resistors, respectively. These elements
 cooperate to generate a constant current i having
 desired temperature characteristics. Further, reference
 10 symbol i_{51} represents a current flowing through the
 resistor R_{51} , i_{52} represents a collector current of
 the bipolar transistor Q_{52} , and i_{53} represents a collector
 current of the bipolar transistor Q_{53} . Before entering
 into discussion about the output current i , description
 15 will first be made on the temperature dependency of
 the value of internal voltage V_{I1} . For the sake of
 simplification, it is assumed in the following descrip-
 tion that the value of the base current of the bipolar
 transistor can be neglected when compared with that
 20 of the collector current thereof and that the collector
 current is approximately equal to the emitter current.
 The voltage V_{I1} can be given by the following expression:

$$V_{I1} = V_{BE}(Q_{51}) + I_{52} \times R_{52} + V_{BE}(Q_{52}) - V_{BE}(Q_{56})$$

..... (4)

where $V_{BE}(Q_{51})$, $V_{BE}(Q_{52})$ and $V_{BE}(Q_{56})$ represent base-

1 emitter forward voltages, respectively. The current I_{52}
 appearing in the expression (4) is given by

$$I_{52} = \{V_{BE}(Q_{55}) - V_{BE}(Q_{54})\}/R_{54} \quad \dots\dots (5)$$

When the current density in the bipolar
 transistor Q_{55} is set at a value n times as large as
 5 that of the bipolar transistor Q_{54} by selecting
 appropriately emitter areas of the bipolar transistors
 Q_{55} and Q_{54} , the following relation applies valid:

$$I_{52} = \frac{1}{R_{54}} \times \frac{kT}{q} \ell_n n \quad \dots\dots (6)$$

In the above expression (6), k represents Boltzmann's
 factor, T represents absolute temperature, and q
 10 represents electron charge. From expressions (4) to
 (6), following relation can be derived:

$$V_{I1} = V_{BE}(Q_{51}) + \frac{R_{52}}{R_{54}} \times \frac{kT}{q} \ell_n n + V_{BE}(Q_{52}) - V_{BE}(Q_{56}) \quad \dots\dots (7)$$

Accordingly, by designing such that the emitter current
 densities of the bipolar transistors Q_{52} and Q_{56} are
 equal to each other, the third and fourth terms in the
 15 right side of the expression (7) are cancelled.

Accordingly,

$$V_{I1} = V_{BE}(Q_{51}) + \frac{R_{52}}{R_{54}} \times \frac{kT}{q} \ell_n n \quad \dots\dots (8)$$

1 Thus, the temperature dependency of the voltage V_{I1} is given by

$$\frac{\partial V_{I1}}{\partial T} = \frac{\partial V_{BE}(Q_{51})}{\partial T} + \frac{R_{52}}{R_{54}} \times \frac{k}{q} \ln n \quad \dots\dots (9)$$

As is well known, the base-emitter voltage of the bipolar transistor exhibits a negative temperature
5 dependency. Accordingly, by varying the ratio n of the emitter current density between the bipolar transistors Q_{55} and Q_{54} or the ratio between the resistance R_{52} and R_{54} , $\partial V_{I1}/\partial T$ given by the expression (9) can be set at an arbitrary value. In view of the fact
10 that the value of V_{I1} obtained at the temperature coefficient set at zero is around 1.2 volt which is substantially equal to the band-gap voltage of the silicon semiconductor, the circuit under consideration is generally referred to as the band-gap generator.

15 In the circuit described above, the collector current of the bipolar transistor Q_{56} is substantially equal to the emitter current thereof. Accordingly, the output current i can be expressed as follows:

$$i = \frac{V_{I1}}{R_{55}} \quad \dots\dots (10)$$

In this way, there can be obtained the output current
20 which has same characteristics as the internal voltage V_{I1} and whose value can be controlled arbitrarily with

1 the aid of the resistor R_{55} .

Employment of the instant embodiment as the constant current supply source in the various embodiments described hereinbefore make possible the control with extremely high stability. In conjunction with the temperature among other, the operation characteristics of the circuit can be controlled in an arbitrary manner by setting the temperature coefficient of the constant current supply source at zero or alternatively at a given positive or negative value.

Further, the internal voltage V_{I1} in the circuit according to the instant embodiment can be made use of as a constant voltage supply of high stability. In this connection, it is noted that unless the constant current output i is required, the output terminal may be connected to the external voltage supply source V_{CC} .

Further, the internal voltage V_{I1} can be utilized as the control voltage V_{CONT}' for the circuit shown in Fig. 20. In that case, it becomes possible to control the temperature characteristic of the differential amplifier.

In the foregoing, the circuit characteristic control method according to the invention has been described in conjunction with several illustrative embodiments. Certainly, these embodiments can be easily realized. However, when the fine (small) elements are used for the realization with a view to increasing

1 the integration density (bit density), there may arise
such situation in which difficulty is encountered in
applying directly the external voltage V_{CC} because of
rather small dielectric (dioxide) breakdown strength of
5 the fine elements. Besides, variation in the external
voltage may make it difficult to obtain the desired
characteristics. Under the circumstance, it is
preferred to generate the stable internal voltage V_I
on chip and use that voltage V_I in place of V_{CC} , as
10 with the case of the embodiments shown in Figs. 4, 5
and 16. Of course, if application of the external
voltage V_{CC} is accompanied with no problems, the external
voltage V_{CC} may be utilized. In this case, the burden
imposed on the voltage supply source generating the
15 internal voltage V_I can be correspondingly reduced,
whereby the internal voltage V_I can be maintained to
be stable. Fig. 34 shows an exemplary embodiment for
controlling the operation speed of the circuit in which
the internal voltage V_I is utilized. Although the
20 following description is based on the assumption that
the CMOS inverter shown in Fig. 11 is controlled by
the circuits shown in Figs. 21 and 22, respectively, it
should be understood that the teaching of the invention
elucidated below can be applied to other various
25 embodiments described hereinbefore. Referring to Fig.
34, P-channel MOS transistors T_{P2} and T_{PR} and N-channel
MOS transistors T_{N2} and T_{NR} constitute a current
mirror circuit. Thus, by selecting appropriately the

1 size of the transistor T_{P2} relative to that of T_{PR} as
in the case of the foregoing embodiments, the charge
current of the driver circuit DRIV can be set at an
arbitrary value. Further, by determining appropriately
5 the size of the transistor T_{N2} relative to T_{NR} , the
discharge current can be set at an arbitrary value.
When source voltage of the P-channel MOS transistors
 T_{PR} and T_{P2} and the voltage V_I of the current supply
source CC2 are held at a value lower than the voltage
10 level which the small or fine elements can withstand,
the latter can of course be used. Further, since the
output amplitude is V_I , the voltage inputted to a
succeeding stage can be controlled stably, whereby
the stable operation of the succeeding stage can be
15 assured. Additionally, it should be mentioned that the
control voltage (V_{CONT} , V_{CONT}') generating circuits
31 and 32 can be used in common among a plurality of
circuits. In that case, the operation speed of the
individual circuits can be controlled as desired by
20 setting the sizes of the associated MOS transistors
 T_{P2} and T_{N2} for every circuit separately. Next,
description will be made of a voltage transformer
circuit suited advantageously for generating a voltage
lower than the external voltage V_{CC} within the body of
25 chip as in the case of the circuits shown in Figs. 4,
5, 34 and others.

Fig. 35 shows a circuit configuration of
the voltage transformer (limiter) circuit 35 according

1 to an embodiment of the present invention. In the
figure, a reference character A denotes generally a
voltage transformer circuit, F denotes a constant
voltage generating circuit, and G denotes an amplifier.
5 The constant voltage generating circuit F is adapted
to generate a constant voltage V_{I1} from the external
supply voltage V_{CC} . The amplifier G amplifies the
voltage V_{I1} to output a voltage V_I of the value required
by the internal circuit 2 or by a circuit portion 3A
10 of the control circuit 3 onto the control line 5I.
It should be mentioned that the voltage V_I may be
imparted with various characteristics through the
constant voltage generating circuit F and the amplifier
G. By compensating, for example, the temperature
15 dependency and the external supply voltage dependency,
the output amplitude of the circuit such as the circuit
shown in Fig. 34 can be made constant independent of
the temperature, whereby the circuit operation of high
stability can be realized. According to the instant
20 embodiment, the output voltage V_{I1} of the constant
voltage circuit can be amplified to a desired value
through the amplifier G. In other words, the value
or level of the voltage V_I can be set without being
limited to the value of the output voltage V_{I1} of the
25 constant voltage circuit.

Fig. 36 shows another embodiment of the
voltage transformer circuit which differs from the
circuit shown in Fig. 35 in that the amplifier GD and

1 a feedback circuit H are provided. The feedback circuit
H is so designed that when the voltage V_I assumes a
desired value, a voltage equal to the constant
voltage V_{I1} is outputted to the output line I_2 . Accord-
5 ing to this embodiment, fluctuation in the output
voltage V_I is fed back through the feedback circuit H,
whereby the value of the output voltage V_I can be
maintained constant with high accuracy even when the
current supplied by way of the control line 5I changes
10 at high speed in the course of time lapse.

Fig. 37 shows a circuit configuration of the
constant voltage generating circuit in the embodiments
shown in Figs. 35 and 36. This constant voltage
generating circuit corresponds substantially to the
15 current supply circuit shown in Fig. 33 except that the
collector of the bipolar transistor is connected to the
external supply voltage V_{CC} . In the circuit shown in
Fig. 37, the output voltage V_{I1} and the temperature
dependency thereof are given by the aforementioned
20 expressions (8) and (9), respectively. As described
hereinbefore, by varying the resistance ratio or current
density ratio of the bipolar transistors, the tempera-
ture dependency can be established. When the instant
embodiment is applied to the constant voltage generating
25 circuits F shown in Figs. 35 and 36, the value of
 $\partial V_{I1} / \partial T$ is so determined as to match with the temperature
characteristics of the amplifier G serving as the dif-
ferential amplifier GD and the feedback circuit H of

1 the succeeding stage, whereby the temperature dependency
of the output voltage V_I of the voltage transformer
circuit can be nullified. It should be noted that in
the circuit arrangement shown in Fig. 31, the voltage
5 V_{I1} remains substantially constant independent of the
external voltage V_{CC} when the latter exceeds a value
about twice as high as that of the base-emitter forward
voltage of the bipolar transistor, i.e. about 1.8 volt.
Accordingly, by applying the instant embodiment to the
10 circuits shown in Figs. 35 and 36, the output voltage
 V_I exhibiting neither the temperature dependency nor
the external voltage dependency can be obtained in a
facilitated and convenient manner.

By the way, it is noted that when the constant
15 voltage circuit F and other circuits are formed simul-
taneously in one and the same semiconductor substrate,
same type of transistors, i.e. either the MOS
transistors or the bipolar transistors should preferably
be used in view of the simplification of the fabrication
20 process and reduction in the manufacturing cost.

For this reason, it may be desirable to use the MOS
transistors in implementing the constant voltage
circuit F rather than the bipolar transistors as in
the case of the embodiment shown in Fig. 37. In that
25 case, the voltage V_{I6} in a circuit corresponding to
the one shown in Fig. 32 except that the drain of the
MOS transistor T_{N63} is connected to the external
supply voltage V_{CC} may be made use of. Alternatively,

1 a constant voltage generating circuit described in
Oguey's article in "Journal of Solid-State Circuit",
SC-15, June 1980 or Blauschild's article in "Journal
of Solid-State Circuit", SC-13, Dec. 1978 may be
5 used.

Fig. 38 shows concretely a circuit configura-
tion of the differential amplifier GD constituting a
part of the circuit shown in Fig. 36.

Referring to Fig. 38, the output voltage
10 V_{I1} of the constant voltage circuit F is applied to
the terminal I_1 while the output voltage V_{I2} of the
feedback circuit is applied to the terminal I_2 . In the
case of the instant embodiment, since the terminals
 I_1 and I_2 correspond to the base electrodes of the
15 bipolar transistors, respectively, gain can be
increased while fluctuation in the voltage V_I can be
suppressed to a negligible level. Parenthetically,
the P-channel MOS transistors in the circuit shown in
Fig. 38 may be replaced by resistors, as is shown in
20 Fig. 39. Since the resistor can be constituted by the
base diffusion layer of the bipolar transistor, this
resistor can be realized within an impurity layer for
the collector of the bipolar transistor. Thus, the
layout area of the circuit can be decreased.

25 As the current source for the differential
amplifiers shown in Figs. 38 and 39, there may be
conceived various types of circuits. It is however
possible to realize the current source circuit with a

1 single MOS transistor, as is illustrated in Figs. 40
 and 41. More specifically, the gates of the MOS
 transistors T_{I61} and T_{I71} are connected to the terminal
 I_1 . With this circuit arrangement, the current of
 5 the differential amplifier can be held constant
 independent of the external voltage V_{CC} , since V_{I1}
 assumes a constant value for V_{CC} , as described herein-
 before. Further, when the characteristics of the
 differential amplifier need to be controlled stably,
 10 various controls may be performed with the aid of the
 circuit shown in Figs. 18 to 20.

Fig. 42 shows more concretely a circuit
 configuration of the feedback circuit shown in Fig. 36.

Referring to Fig. 42, for the voltage V_I on
 15 the control line 5I, there is produced at an output
 terminal I_2 a voltage V_{I2} which can be given by

$$V_{I2} = \frac{R_{82}}{R_{81} + R_{82}} \times V_I \quad \dots\dots (11)$$

The above-mentioned voltage V_{I2} is inputted to the
 differential amplifier shown in Fig. 36. Accordingly,
 when the resistance values of resistors R_{81} and R_{82}
 20 are so selected that the following condition is met

$$V_{I1} = \frac{R_{82}}{R_{81} + R_{82}} \times V_{I0} \quad \dots\dots (12)$$

(where V_{I1} represents the output voltage of the constant

1 voltage circuit F and V_{I0} represents a desired voltage
to be outputted onto the control line 5I), then, $V_{I1} =$
 V_{I2} provided that $V_I = V_{I0}$, which means that the
voltage on the control line 5I is stabilized at the
5 desired voltage V_{I0} . By designing the constant voltage
circuit F so that the temperature dependency of the
output voltage V_{I1} thereof is nullified, as described
hereinbefore, the temperature dependency of the above-
mentioned voltage V_{E0} can be substantially nullified.

10 Needless to say, it is also possible to
impart a desired temperature dependency to the output
voltage V_{I0} , if required.

Fig. 43 shows concretely a circuit configura-
tion of the feedback circuit H shown in Fig. 36.

15 In the case of the embodiment shown in Fig. 43, the
control line 5I is not directly connected to the
resistor but connected to the base electrode of the
bipolar transistor Q_{91} . Accordingly, owing to the
current amplification by the bipolar transistor Q_{21} ,
20 circuit operation of higher speed can be realized when
compared with the circuit shown in Fig. 42. Further,
the load current of the differential amplifier GD can
be decreased. In the case of the circuit shown in
Fig. 43, the aforementioned expressions (11) and (12)
25 have to be rewritten as follows:

$$V_{I2} = \frac{R_{92}}{R_{91} + R_{92}} \{V_I - V_{BE}(Q_{91})\} \quad \dots\dots (13)$$

$$V_{I1} = \frac{R_{92}}{R_{91} + R_{92}} \{V_{I0} - V_{BE}(Q_{91})\} \quad \dots\dots (14)$$

- 1 The values of the resistors R_{91} and R_{92} are so determined that the condition given by the expression (14) can be satisfied. However, since

$$V_{I0} = \frac{R_{91} + R_{92}}{R_{92}} V_{I1} + V_{BE}(Q_{91}) \quad \dots\dots (15)$$

- as is apparent from the expression (14), the temperature dependency of the voltage V_{I0} is out of coincidence with that of the voltage V_{I1} because of the second term in the expression (15). In this case, from the expression (11)

$$\frac{\partial V_{I0}}{\partial T} = \frac{R_{91} + R_{92}}{R_{92}} \times \frac{\partial V_{I1}}{\partial T} + \frac{\partial V_{BE}(Q_{91})}{\partial T} \quad \dots\dots (16)$$

- Accordingly, the circuit can be designed in accordance with the desired V_{ID} and $\partial V_{I0}/\partial T$ so that the conditions given by the expressions (15) and (16) are satisfied. Of course, the term $\partial V_{I0}/\partial T$ may be nullified.

- With the voltage transformer circuits described above, the output voltage can be maintained at a constant value lower than the external voltage V_{CC} even when the latter is increased excessively, whereby the fine elements or devices can be protected

1 against destruction, to a great advantage. However,
there may arise such problem that the circuit can not
be subjected to the aging test. This will be elucidated
below.

5 Conventionally, the integrated circuits
usually undergo the so-called aging test after the
final fabrication step, wherein a higher voltage than
that used in the ordinary operation are intentionally
applied to the individual transistors implemented
10 within the integrated circuit for finding out at
earlier stage those transistors inherently susceptible
to failure due to defect in the gate oxide film for
thereby enhancing the reliability of the products.
In order to increase the possibility of finding out the
15 failed product through the aging test, such a voltage
which is slightly lower than the voltage at which a
normal element or device would be destroyed has to be
applied to the individual elements or device. In this
connection, it is noted that in the case of the integrated
20 circuit chip realized such that a predetermined source
voltage is supplied by way of the on-chip voltage
transformer (limiter) circuit, there may arise such a
case in which adequate aging test voltage can not be
applied to the internal circuitries. This problem
25 can however be solved by designing the voltage
transformer (limiter) circuit such that the voltage V_I
generated thereby is increased when the external power
supply voltage V_{CC} assumes an excessively high level.

1 More specifically, referring to Fig. 44, the internally
generated voltage V_I is held at a constant value V_{I0}
when the external power supply voltage lies within
a range of V_{CI} to V_{CE} , while the internal voltage V_I
5 is increased as the external power supply voltage V_{CC}
is increased beyond the level V_{CE} . In this way,
when the external power supply voltage V_{CC} is increased
beyond the level V_{CE} , the internal voltage V_I can be
increased. Accordingly, a voltage higher than the
10 constant internal voltage level V_{I0} can be applied to
the on-chip circuitries by increasing the external
power supply voltage V_{CC} beyond the level V_{EC} in the
aging test, which test thus can be carried out
effectively.

15 Fig. 45 shows concretely a circuit arrangement
for realizing the voltage characteristics illustrated
in Fig. 44. Referring to Fig. 45, the constant
voltage generating circuit F is similar to the circuit
shown in Fig. 37 except for the differences mentioned
20 below. Namely, a resistor R_{111} is inserted between
the collector of the bipolar transistor in the output
stage J and the terminal D. The differential amplifier
CD and the feedback circuit H are interconnected in
the same manner as in the case of the circuit shown
25 in Fig. 36.

Additionally, the collector of the bipolar
transistor Q_{111} is connected to the base of the bipolar
transistor Q_{112} . The emitter of the latter is connected

1 to the control line 5I with the collector thereof being
coupled to the external power supply voltage V_{CV} . With
this circuit arrangement, the output voltage V_I remains
constant at the value V_{I0} until the bipolar transistor
5 Q_{112} is turned on after the external power supply
voltage V_{CC} has reached the stable point V_{I0} of the
output voltage V_I , which is increased as the external
voltage V_{CC} increases after the bipolar transistor
 Q_{112} has been turned on. The point V_{CE} at which the
10 bipolar transistor Q_{112} is turned on is given by the
following expression:

$$V_{CE} = V_{I0} + V_{BE}(Q_{112}) + R_{111} \times i_{11} \quad \dots\dots (17)$$

where i_{11} represents a current flowing through the
resistor R_{111} and satisfies the condition given by the
following expression:

$$i_{11} = V_{I1}/R_{112} \quad \dots\dots (18)$$

15 Accordingly,

$$V_{CE} = V_{I0} + V_{BE}(Q_{112}) + \frac{R_{111}}{R_{112}} V_{I1} \quad \dots\dots (19)$$

When the external power supply voltage V_{CC} increases
beyond the level or point V_{CE} , the internal voltage
 V_I increases, as is given by the following expression:

$$\begin{aligned}
V_I &= V_{CC} - R_{111} \times i_{11} - V_{BE}(Q_{112}) \\
&= V_{CC} - \frac{R_{111}}{R_{112}} V_{I1} - V_{BE}(Q_{112}) \quad \dots\dots (20)
\end{aligned}$$

1 In this way, since the voltage V_I increases as the external voltage V_{CC} is increased after the latter exceeds the level V_{CE} , the aforementioned aging test can be carried out effectively.

5 Parenthetically, when the temperature dependency of the voltage level V_{I0} is nullified, then the voltage level V_{CE} is given from the expression (19) as follows:

$$\frac{\partial V_{CE}}{\partial T} = \frac{\partial V_{I0}}{\partial T} + \frac{\partial V_{BE}(Q_{112})}{\partial T} + \frac{R_{111}}{R_{112}} \times \frac{\partial V_{I1}}{\partial T} \quad \dots\dots (21)$$

On the other hand, when $V_{CC} > V_{CE}$, the temperature
10 dependency of the voltage V_I is given by the following expression:

$$\frac{\partial V_I}{\partial T} = - \frac{R_{111}}{R_{112}} \times \frac{\partial V_{I1}}{\partial T} - \frac{\partial V_{BE}(Q_{112})}{\partial T} \quad \dots\dots (22)$$

When the circuit shown in Fig. 42 is used as the feed-back circuit, $\partial V_{I1}/\partial T = 0$ from the expression (12). Accordingly

$$\frac{\partial V_{CE}}{\partial T} = \frac{\partial V_{BE}(Q_{122})}{\partial T}$$

When $V_{CC} > V_{CE}$

$$\frac{\partial V_E}{\partial T} = - \frac{\partial V_{BE}(Q_{112})}{\partial T}$$

- 1 Usually, the temperature dependency of the voltage V_{BE} is about $-2\text{mV}/^\circ\text{C}$. Accordingly, the temperature dependency of the voltage V_{CE} as well as that of V_I is extremely small when $V_{CE} > V_{CC}$. Further,
- 5 when the circuit shown in Fig. 43 is employed as the feedback circuit, the following expression applies valid from the expression (14) provided that $\partial V_{I0}/\partial T = 0$:

$$\frac{\partial V_{I1}}{\partial T} = \frac{-R_{92}}{R_{91} + R_{92}} \times \frac{\partial V_{BE}(Q_{91})}{\partial T}$$

Accordingly, from the expressions (21) and (22)

$$\frac{\partial V_{CE}}{\partial T} = \frac{\partial V_{BE}(Q_{112})}{\partial T} - \frac{R_{111} \times R_{92}}{R_{112}(R_{91} + R_{92})} \times \frac{\partial V_{BE}(Q_{91})}{\partial T}$$

..... (23A)

When $V_{CC} > V_{CE}$

$$\frac{\partial V_I}{\partial T} = \frac{R_{111} \times R_{92}}{R_{112}(R_{91} + R_{92})} \times \frac{\partial V_{BE}(Q_{91})}{\partial T} - \frac{\partial V_{BE}(Q_{112})}{\partial T}$$

..... (23B)

1

From the expressions (11) and (15),

$$\begin{aligned}
 V_{CE} &= V_{I0} + V_{BE}(Q_{112}) + \frac{R_{111}}{R_{112}} \\
 &\quad \times \frac{R_{92}}{(R_{91} + R_{92})} \{V_{I0} - V_{BE}(Q_{91})\} \\
 &= (1 + \eta)V_{I0} + V_{BE}(Q_{112}) - \eta V_{BE}(Q_{91}) \quad \dots\dots (23C)
 \end{aligned}$$

where

$$\eta = \frac{R_{111}}{R_{112}} \times \frac{R_{92}}{R_{91} + R_{92}}$$

Thus, assuming, by way of example, that $V_{CE} = 6$ V and $V_{I0} = 4$ V, then $V_{BE}(Q_{112}) = V_{BE}(Q_{91}) = 0.8$ V. Thus, $\eta = 3/8$. From the expressions (23A) and (23B), the values of $\partial V_{CE}/\partial T$ and $\partial V_E/\partial T$ when $V_{CC} > V_{CE}$ are about -1.25 mV/ $^{\circ}$ C and about $+1.25$ mV/ $^{\circ}$ C, respectively. This means that even when the circuit shown in Fig. 43 is employed as the feedback circuit H, the temperature dependency of the voltage level V_{CE} as well as that of V_E when $V_{CC} > V_{CE}$ is very small. Further, by selecting the value of V_{CE} about twice as large as the value of V_{I0} when the circuit shown in Fig. 43 is employed, the temperature dependency of V_{CE} and that of V_I when $V_{CC} > V_{CE}$ can be simultaneously made approximately zero. More specifically, when $V_{BE}(Q_{112}) \approx V_{BE}(Q_{91})$, $V_{CE} \approx 2V_{I0}$ from the expression (23C) provided that $\eta = 1$. Thus, when

$$\frac{\partial V_{BE}(Q_{91})}{\partial T} \approx \frac{\partial V_{BE}(Q_{112})}{\partial T}$$

1 then $\partial V_{CE}/\partial T \approx 0$ from the expression (23a). Similarly,
 $\partial V_I/\partial T \approx 0$ from the expression (23B) when $V_{CC} > V_{CE}$.

As will now be appreciated from the foregoing,
the voltage characteristics illustrated in Fig. 44 can
5 be realized without undergoing any appreciable
influence of fluctuation in the temperature by using
the circuit shown in Fig. 42 or the circuit shown in
Fig. 43 as the feedback circuit H. As a result of
this, the voltage V_I exhibiting substantially no
10 temperature dependency can be generated not only in
the ordinary operation range of $V_{CC} \leq V_{CE}$ but also in
the aging test range of $V_{CC} > V_{CE}$, whereby the internal
circuitries can be operated stably.

Of course, it is possible to impart the temper-
15 ature dependency to the voltage V_{I0} , if demanded, as
described hereinbefore. Further, when it is required
to set the temperature dependency in the aging test
range independent of the voltage V_{I0} , this can be
achieved by connecting the collector of the bipolar
20 transistor Q_{111} to the external power supply voltage
 V_{CC} while providing the resistor R_{111} having a desired
temperature dependency for the bias K separately from
the feedback circuit F, as is shown in Fig. 45.

In the circuit shown in Fig. 45, the bipolar
25 transistor Q_{112} is employed for rising the internal

1 voltage V_I when $V_{CC} \geq V_{CE}$. However, this transistor
may be replaced by an N-channel MOS transistor, wherein
the gate of that N-channel MOS transistor is connected
to the terminal K while the drain thereof is connected
5 to the external power supply V_{CC} with the source of
that transistor being connected to the terminal E.
Since the terminal K is connected to the gate of the
N-channel MOS transistor, there is required no current
supply, whereby the design of the constant voltage
10 generating circuit can be facilitated correspondingly.

According to the embodiment of the invention
described above, it is possible to supply a stable
voltage having a desired temperature dependency to
the control line 5I within a desired range independent
15 of the external power supply voltage, which in turn
means that the circuits implemented on one and the
same chip can be operated stably. However, when the
current supplied through the control line 5I is
especially large, a buffer circuit for amplification
20 of current may be provided in the voltage transformer
circuit A, wherein the output line 5I' of the buffer
circuit may be made use of as the control line for
preventing fluctuation in the voltage.

Fig. 46 shows an exemplary embodiment of
25 the above-mentioned buffer circuit, wherein C_{121} and
 C_{122} designate capacitors for suppressing fluctuation
in potential on the control line 5I'. In this circuit,
the output voltage V_I' on the control line 5I' can be

1 expressed as follows:

$$V_I' = V_{CC} - V_{BE}(Q_{121}) \quad (V_{CC} \leq V_I + V_{BE}(Q_{121}))$$

..... (24)

or

$$V_M = V_I + V_{BE}(Q_{121}) - V_{BE}(Q_{122}) \quad (V_{CC} > V_I + V_{BE}(Q_{121}))$$

..... (25)

The voltages V_I' and V_I (internal voltage) are substantially equal to each other in the range given by

$$V_{CC} \geq V_I + V_{BE}(Q_{121})$$

..... (26)

The temperature dependency of the output voltage V_I' can
5 be controlled by employing the aforementioned embodiment
as the circuit for generating the internal voltage V_I .
In the circuit under consideration, the control line
5I' is connected to the emitter of the bipolar transistor.
Thus, it is possible to supply a large current through
10 the control line 5I'. In other words, the voltage V_I'
can be held stably even when a large current is
supplied to the on-chip circuit.

Figs. 47 shows another embodiment of the
buffer circuit which differs from the one shown in
15 Fig. 46 in that the bipolar transistor is replaced
by the MOS transistor. With the circuit configuration
shown in Fig. 47, the voltage V_I' is substantially
equal to the internal voltage V_I in the range given by

$$V_{CC} \geq V_I + V_{TH}(Q_{132}) \quad \dots\dots (27)$$

1 where V_{TH} represents the threshold voltage of the MOS transistor.

Since the threshold voltage of the MOS transistor can be easily controlled, it is possible
 5 according to this embodiment to stabilize the output voltage V_I' starting from the state in which the external voltage V_{CC} is still at a low level, by making the output voltage V_I' equal to the internal voltage V_I .

In the case of both embodiments of the buffer
 10 circuit described above, the range of the external voltage V_{CC} in which the internal voltage V_I and the output voltage V_I' become equal to each other is limited by the forward voltage in the base-emitter path of the bipolar transistor or by the threshold voltage of
 15 the MOS transistor. Accordingly, even when the circuit shown in Fig. 46 is designed such that the output voltage V_I of the voltage transformer circuit becomes constant at 4 volts with the external voltage V_{CC} being equal to or higher than 4 volts, by way of example,
 20 the output voltage V_I' of the buffer circuit shown in Fig. 46 can not become constant at 4 volts unless the external voltage becomes equal to or higher than about 4.8 volts. As a consequence, the operation margin of the internal circuitries relative to the
 25 external voltage V_{CC} may possibly be narrowed. For coping with this problem, the buffer circuit of such

1 configuration as shown in Fig. 48 may be employed.
In the circuit shown in Fig. 48, the control line 5I'
is connected to a drain electrode of a P-channel MOS
transistor M141 having a source electrode connected
5 to the external power supply voltage V_{CC} , while the
gate G141 of the MOS transistor is connected to the
output of a differential amplifier Q so as to be
controlled by the output voltage thereof. The input
terminal of the differential amplifier Q is supplied
10 with the output voltage V_I of the voltage transformer
(limiter) circuit A and the output voltage V_I' of the
buffer circuit under consideration. The capacitor
 C_{141} serves for suppressing fluctuation in the output
voltage V_I' . With this circuit arrangement, the output
15 voltage V_I' can be held at a value equal to the voltage
 V_I by means of the differential amplifier mentioned
above. Thus, in contrast to the buffer circuits
shown in Figs. 46 and 47, the output voltage V_I' can be
made equal to the internal voltage V_I independent
20 of the external voltage V_{CC} in the case of the embodi-
ment shown in Fig. 48, whereby a stable voltage can
be derived over a wide range of the external voltage
 V_{CC} .

Fig. 49 shows a concrete example of the
25 circuit configuration for the circuit shown in Fig. 48.
Referring to Fig. 49, terminals P and \bar{P} are supplied
with signals of opposite phases, respectively. Although
it is assumed in the following description that the

1 signal P is of high level with the signal \bar{P} being low
level, essential same effect can be obtained even
when the relation in level between these signals
is reversed. Further, in the following description,
5 the external voltage V_{CC} is assumed to be 5 volts with
the internal voltage V_I being 4 volts, it goes without
saying that other voltage values may also be used
within the purview of the invention. Additionally,
for the sake of simplification of description, the
10 base-emitter voltage of the bipolar transistor is assumed
to be 0.8 volt. When the internal voltage V_I is 4
volts, the base potential V_{B153} of the bipolar
transistor Q_{153} is 1.6 volts. At that time, the
potential V_I' on the control line 5I' assumes the base
15 potential V_{B154} of the bipolar transistor Q_{154} , i.e.
1.6 volts. When the potential V_I' on the control
line 5I' is lowered, the collector current of the
bipolar transistor Q_{154} is decreased. On the other
hand, the collector current of the bipolar transistor
20 Q_{153} is increased, which results in that the current
flowing through a resistor R_{151} is increased.
Consequently, the gate potential V_{GM141} of the MOS
transistor T_{M141} is lowered, whereby the drain current
of the MOS transistor T_{M141} is increased, as the
25 result of which the voltage V_I' is restored to 4 volts.
Reversely, when the voltage V_I' rises up, the gate
potential V_{GM141} becomes high, causing the MOS transistor
 T_{M141} to be turned off. Thus, the voltage V_I' is lowered

1 to restore 4 volts. In this connection, it should be
mentioned that the collector potential of the bipolar
transistor Q_{153} is prevented from being lowered below
2.6 volts because of a series connection of diodes
5 D_{153} to D_{155} inserted between the collector of the
transistor Q_{153} and the external power supply V_{CC} . On
the other hand, since the base potential V_{B153} is
1.6 volts, the base potential of the bipolar transistor
 Q_{153} always remains lower than the collector potential.
10 Thus, the bipolar transistor Q_{153} will never become
saturated. The base potential of the bipolar transistor
 Q_{154} is at $(V_I' - 2.4)$ volts with the collector
potential thereof being $(V_{CC} - 2.4)$ volts. Since the
internal voltage V_I is ordinarily lower than the
15 external voltage V_{CC} , the bipolar transistor Q_{154} will
never be saturated. By the way, when the circuit
connected to the control line $5I'$ is in the standby
state, the current flowing through the control line
 $5I'$ is substantially constant at a small value in most
20 cases. In this state, the internal voltage V_I can
be maintained constant even when the current flowing
to the amplifier is decreased, which in turn means
that the power consumption can be reduced by decreasing
the current flowing through the amplifier. To this
25 end, however, the resistance value of the resistor
 R_{152} has to be selected greater than that of the
resistor R_{151} , while the gate widths of the MOS
transistors T_{M153} , T_{M154} and T_{M155} have to be selected

1 greater than those of the MOS transistors T_{M156} , T_{M157}
and T_{M158} , respectively. Besides, the potentials at
the terminals P and \bar{P} have to be changed over to low
and high levels, respectively, when the circuit
5 connected to the control line 5I' is in the standby
state.

It should be mentioned here that the output
 V_I or V_I' of the voltage transformer (limiter)
circuits described above by reference to Figs. 35
10 to 49 may also be utilized as the control voltage
 V_{CONT} for the circuits shown in Figs. 7 to 10. Since
the fluctuations in the output voltage V_I and V_I' due
to the variations in temperature and the external
voltage can be controlled with the circuits shown in
15 Figs. 35 to 49, the characteristics of the circuits
shown in Figs. 7 to 10 can be maintained constant
independent of the external voltage and the temperature.
Thus, the circuits shown in Figs. 35 to 49 are
advantageously effective for solving the problem
20 brought about by variations or changes in the external
voltage V_{CC} and the temperature in particular.

Fig. 50A shows a concrete circuit configura-
tion of the basic arrangement schematically shown in
Fig. 2. The circuit shown in Fig. 50 is so arranged
25 as to detect a phase difference in time Δt between
two predetermined pulses ϕ_1 and ϕ_2 in the circuit 2
for thereby controlling the operation of the circuit
2 so that the operating speed is maintained constant.

1 In Fig. 50A, F/F designates a set-reset type
flip-flop adapted to produce the pulse signal ϕ_1 having
a pulse width (duration) equal to the time difference
between the pulse signals ϕ_1 and ϕ_2 . Reference
5 symbols SW_I , SW_R and SW_S designate switches, respec-
tively, C_I and C_H designate capacitors and V_{REF} represents
a voltage for reference. Operation of the circuit shown
in Fig. 50A will be described by reference to Fig.
50B.

10 In response to the input of the signal ϕ_1 ,
a pulse signal ϕ_I is outputted, whereupon the switch
 SW_I is turned on to cause the capacitor C_I to be
charged with a constant current i , resulting in that
the voltage at the terminal 31 of the capacitor C_I
15 rises up progressively. When the pulse signal ϕ_2 is
inputted after time lapse of Δt , the signal ϕ_I assumes
a low potential level, whereupon the switch SW_I is
turned off. Consequently, a voltage V_{HL} at a circuit
point 31 assumes a value proportional to the time or
20 phase difference Δt . This voltage V_{HL} is charged in
the capacitor C_H when the switch SW_S is turned on in
response to the inputting of a pulse signal ϕ_S . By
dimensioning the capacitances of the capacitors C_I
and C_H such that $C_I \gg C_H$, the voltage at the circuit
25 point +32 becomes substantially equal to the voltage
 V_{HL} . On the other hand, the capacitor C_I is discharged
to zero volt in preparation for the succeeding operation
when the switch SW_R is turned on in response to a pulse

1 signal ϕ_R . The voltage V_{HL} stored in the capacitor
C_H is compared with the reference voltage V_{REF} through
an operational amplifier 7, whereupon a voltage
corresponding to the resultant difference is outputted
5 onto the line 5 for controlling the operation
characteristics of the circuit 2 which may be imple-
mented in such circuit configuration as shown in
Figs. 7 to 20 so that the operation characteristics
thereof are varied in dependence on the voltage on the
10 line 5 until the voltage value V_{HL} ultimately becomes
equal to the reference voltage V_{REF} . In this manner,
the characteristics of the circuit 2 is maintained to
be constant.

With the arrangement according to the instant
15 embodiment, the characteristics of the circuit 2 is
controlled by detecting directly the operation
characteristics of the circuit 2. Accordingly,
response can be made even to variations in other
characteristics than those previously taken into
20 consideration. Thus, the characteristics of the
circuit 2 can be controlled with an extremely high
accuracy. In the case of the instant embodiment, the
reference voltage V_{REF} and the current i mainly determine
the control accuracy and are thus required to be highly
25 stable. In this connection, the reference voltage
 V_{REF} can be produced with the aid of the circuits shown
in Figs. 32 and 37, while the current i of such high
stability can be produced with the circuits shown in

1 Figs. 26 and 33, respectively.

Although the operation characteristics of the circuit 2 are detected in terms of time (phase) difference between the pulse signals ϕ_1 and ϕ_2 , it
5 is equally conceivable to perform the characteristic control on the basis of other detected quantities such as, for example, operation current.

Fig. 51 shows an embodiment corresponding to the one shown in Fig. 50 applied to the basic arrange-
10 ment shown in Fig. 3. According to this embodiment, a dummy circuit 4 is constituted by a part of the internal circuitry 2' constituting the circuit 2, wherein the operation characteristics are detected with the aid of outputs ϕ_1' and ϕ_2' of the dummy circuit 4 and
15 controlled in the manner similar to that described above in conjunction with Fig. 50. The dummy internal circuitry 2' may be implemented in the form of a ring oscillator by using an inverter such as shown in Fig. 7 or any other suitable circuits. This embodiment
20 provides similar advantageous effects as those attained with the circuit shown in Fig. 50.

Of the embodiments described above, the circuit shown in Fig. 12, for example, is so arranged that the base and collector currents of the bipolar
25 transistor are supplied from the same power supply source. In that case, there may arise such a situation that the collector potential is temporarily lowered below the base potential due to voltage drop appearing across

1 the collector resistor of the bipolar transistor,
whereby the latter may be driven to the saturated state.
For evading such undesirable situation, two collector
terminals C1 and C2 are provided, wherein the terminal
5 C1 is used as the collector electrode of the bipolar
transistor while the terminal C2 is connected to the
MOS transistor supplying the base current, as is
shown in Fig. 52. With this arrangement, the potential
at the second collector electrode is lower than the
10 that of the inherent collector C0 of the bipolar
transistor, as a result of which the potential at
the base connected to the second collector electrode
by way of the MOS transistor will never become higher
than the potential at the collector C0. In this
15 way, the possibility of the bipolar transistor being
driven into saturation can be positively excluded.
It should be understood that the application of this
embodiment is never restricted to the circuit shown
in Fig. 12.

20 Fig. 53 shows concretely an exemplary arrange-
ment of a dynamic random access memory (DRAM) to which
the embodiments of the invention described above are
applied.

In this figure, a reference symbol MA
25 designates a memory cell array constituted by memory
cells arrayed two-dimensionally. Reference symbol PC
designates a data wire precharge circuit, and SA
designates a sense amplifier for amplifying a feeble

1 signal outputted onto the data wire from the memory
cell, the sense amplifier being constituted by P-
and N-channel MOS transistors. Symbol AB designates
an address buffer circuit for translating an address
5 input A_{in} into an internal signal, "X-Dec & Driv." and
"Y-Dec & Driv." designate an X-decoder driver and a
Y-decoder driver, respectively, DP designates a
generator circuit for generating the data wire precharge
voltage when the memory is in the standby state, SAD
10 and \overline{SAD} designate driver circuits for the sense
amplifier, and WC designates a write control circuit
for writing the data input signal D_{in} into memory
cell under the command of a write-in signal WE. A
peripheral circuit serves for generating pulse signals
15 required for operation of the individual circuit in
accordance with external inputs. A reference symbol
MA denotes a main amplifier for amplifying the read-
out signals on the input/output (I/O) line. The circuit
shown in Fig. 19 may be employed as the main amplifier.
20 A reference numeral 3 designates the circuit for
outputting signals 5 in accordance with deviation or
variation in the fabrication process condition and the
operating condition onto the lines 5 for controlling
operation of the individual circuit so that the
25 characteristics thereof can be maintained stable. The
individual circuits are implemented in the configurations
shown in Figs. 7 to 20 so as to be controlled by the
outputs of the circuit 3.

1 In operation, upon inputting of a signal CE,
the memory read operation is started. The address
input signal A_{in} is amplified by the address buffer
circuit AB to supply the output signal thereof to
5 the decoders X-Dec and Y-Dec. In response thereof, one
word wire W is selected by the associated drivers
"X-Dec & Driv", whereupon information charge stored in
the capacitors of the memory cell is outputted onto the
selected data wire or line, resulting in appearance
10 of a feeble signal on the data line, which signal is
then amplified by the sense amplifier SA. The selected
data wire signal is outputted to the I/O and $\overline{I/O}$ ports
through "Y-Dec & Driv.". This signal is amplified
by the main amplifier MA to be outputted externally as
15 the signal D_{out} . The write operation is performed
through the procedure reverse to the above in response
to the data input signal WC.

With the arrangement described above, controls
may be performed for various purposes.

20 In the first place, there can be mentioned
the control method for maintaining the operation speed
or reliability of the whole circuit to be constant.
To this end, the control circuit 3 can produce the
control signals conforming to the individual circuits
25 in accordance with the fabrication process condition
and the operating condition, which control signals being
outputted to the circuit 5 to be utilized for the
intended controls.

1 A method of controlling the individual circuits
independently in accordance with the functions thereof.
In particular, in the case of the DRAM, the memory
cell array unit is realized by using the finest (smallest)
5 elements and is poor in respect to the dielectric
(dioxide) breakdown strength as compared with the other
circuitries. Under the circumstance, the control of
the memory cell array will be concerned with the
enhancement of reliability, while the control for the
10 other circuits will be for stabilization of the operation
speed and stabilization. The method of controlling
the operation speed can be realized in accordance with
the teachings of the invention incarnated in the
several embodiments thereof described hereinbefore.
15 Concerning the control of the memory array, several
methods are conceivable. As one of them, there can
be mentioned a method of maintaining the electric field
to be constant in the thickness of insulation film of
the capacitor C_S constituting the memory cell. This
20 is because the dielectric breakdown strength of the
capacitor C_S is smallest in the whole chip, since
there is a general trend for minimizing the thickness
 t_{oxs} of the insulation film of the capacitor serving
as dielectric thereof with a view to realizing the
25 element C_S in a large capacitance in a possibly smallest
area because the element C_S should have a large capacitance
for ensuring the stable operation by increasing the
amount of information charge Q_S . In order to ensure

- 1 high reliability by maintaining the electric field
 E_{OXS} to be constant, the output voltages of the sense
 amplifier drive circuit SAD, precharge driver DP,
 write circuit WC and others may have to be controlled
 5 for thereby controlling the voltage V_S at which the
 information is written in the cell element C_S . In
 this connection, the quantity of information charge
 Q_S is expressed as follows:

$$\begin{aligned} Q_S &= C_S \times V_S \\ &= \frac{\epsilon_{\text{OXS}} \times A_{\text{OXS}}}{t_{\text{OXS}}} \times V_S \\ &= \epsilon_{\text{OXS}} \times A_{\text{OXS}} \times E_{\text{OXS}} \end{aligned}$$

- where ϵ represents dielectric constant, and A_{OXS}
 10 represents the area of C_S .

- As will be seen from the above expression,
 the quantity of information charge Q_S can be maintained
 constant by maintaining constant the electric field
 E_{OXS} , whereby reliability as well as stability of
 15 operation can be enhanced. Further, as the temperature
 rises, the diffusion layer leakage current in the memory
 cell MC is decreased. Accordingly, the minimum quantity
 of the information charge required for the stable
 operation has to be also increased. To this end, such
 20 control may be performed for increasing the information
 charge Q_S and hence the electric field E_{OXS} as the

1 temperature becomes higher, to thereby further enhance
the reliability. In this case, since conductance G_m
of the MOS transistor is lowered as the temperature
increases, the control can be accomplished without
5 involving any significant increase in the peak values
of the data line charge/discharge currents.

Further, there can be mentioned a control
method associated with the MOS transistors constituting
other parts of the memory cell MA. The MOS transistor
10 is a finest element on the chip, and in most cases,
the dielectric breakdown strength and the hot-carrier
breakdown strength tend to be smaller when compared
with other elements. The various strength factors
of the MOS transistor are more degraded as the gate
15 length L_g is shorter and as the gate insulation film
thickness t_{oxs} becomes smaller. Accordingly, it is
desirable to lower the voltages applied to the word
wire, data wire and others, as to values of the gate
length L_g and the insulation film thickness t_{oxs} become
20 smaller. To this end, the control of the applied
voltage can be performed by the method similar to
those described hereinbefore. Besides, the hot carrier
breakdown strength also becomes lowered as the tempera-
ture decreases. Accordingly, the voltages on the
25 data wire and others may have to be lowered as the
temperature becomes lower. Through this control, there
can be realized the high stable and reliable charac-
teristics. Needless to say, the control method described

1 just above may be combined with the control method
concerning with the memory cell capacitance C_S .

As will be appreciated from the above
description, operation of the DRAM can be controlled
5 in association with various factors. In the case of
the DRAM, the prevailing trend is to implement the
constituent element in more and more small size in an
effort to realize the higher integration bit density.
At present, the external power supply voltage V_{CC} of
10 5 volts is used, it is expected in the future that
difficulty will be encountered in applying the voltage
of 5 volts directly to the fine elements in view of
degradation in the voltage withstanding capability
thereof as the integration bit density is increased
15 from 4 Mbits and hence to 16 Mbits. However, a smaller
value of the voltage V_{CC} than 5 volts is not preferred
when taking into consideration the compatibility with
the conventional DRAMs, because otherwise a burden is
imposed on the user. Accordingly, it is also preferred
20 in the case of DRAM that a lower voltage than V_{CC} is
generated by the control circuit such as shown in
Figs. 4 and 5 to thereby protect the fine constituent
elements of the DRAM in performing the various controls.

Fig. 54 shows an exemplary embodiment of
25 the control circuit according to the invention which
incorporates therein the power supply circuit mentioned
above. In this figure, reference symbol 511' denotes
a control line for supplying a voltage V_I' lower than

1 V_{CC} to peripheral circuits such as address buffer,
decoder, clock driver and the like, 5I2 denotes a
control line for supplying voltage V_{CH} higher than
 V_I' to a word driver circuit, 5I3H and 5I3L denote
5 control lines for controlling driver circuits SAD
and \overline{SAD} for the sense amplifier SA. It goes without
saying that the control circuit 3 shown in Fig. 54
includes other circuitries as required for the control,
although they are omitted from illustration. Further,
10 in Fig. 54, reference symbol F denotes a constant voltage
generating circuit for generating a stable reference
voltage suited for the aging test, Q_{112} denotes a
bipolar transistor, GD denotes a comparator, H denotes
a feedback circuit, Q denotes a comparator for supplying
15 the voltage V_I' lower than V_{CC} to the address buffer,
decoder, the clock drivers and the like on the basis
of the reference voltage V_I' , T_{M141} denotes a MOS
transistor, HOP denotes a high voltage generating circuit
for supplying a higher voltage V_{CH} than V_I' to the
20 word driver and others for operation, V_{st} denotes a
high voltage generating circuit for generating a high
voltage in the standby state, and DRV and DRV' denote
driver circuits for controlling a data wire voltage
 V_O and a data wire current, respectively. With the
25 arrangement shown in Fig. 54, the voltages V_I' and V_I
are equal to each other. Besides, the voltages V_{CH}
and V_O are determined on the basis of the voltage
 V_I' . Accordingly, all the internal voltage within the

1 DRAM can be controlled on the basis of the voltage V_I .
Thus, the memory cell array and the peripheral circuits
according to the preceding embodiment can be positively
protected against variation in the characteristics
5 regardless of fluctuation in the external voltage V_{CC}
and temperature, whereby the DRAM enjoying extremely
stable operation can be realized. The aging test can
of course be carried out effectively. In case the
circuit shown in Fig. 37 or 45 is employed as the
10 constant voltage circuit F in the control circuit 3
shown in Fig. 54, power consumption can be reduced in
the manner elucidated below. In the constant voltage
circuit F shown in Figs. 37 and 45, the output voltage
 V_{I1} is determined by the resistance ratio, as will
15 be seen from the expression (15). Besides, the aging
voltage characteristics are also determined by the
resistance ratio, as can be seen from the expression
(20). In this way, the characteristics undergo no
variation independent of change in the absolute value
20 of the resistances, which in turn means that the
characteristics is less susceptible to the influence
of deviations in the fabrication process condition.
Accordingly, it is possible to set only the current
at a desired value with the resistance ratio being left
25 unchanged, by multiplying the absolute values of
resistors uniformly with a factor Z (Z is greater than
zero). In case the current value is decreased, noise
generated by other circuit implemented on the same

1 semiconductor substrate may provide an influential
factor. This problem can be solved by increasing the
current flowing to the reference voltage generating
circuit F when the semiconductor device including this
5 circuit F is in the operating state, to thereby prevent
fluctuation in the voltage brought about by noise or
other transients, while in the standby state, the
current is decreased for the purpose of reducing the
power consumption. Figs. 55 and 56 show concrete
10 examples of the circuit designed to this end. Referring
to Fig. 55, a P-channel MOS transistor is provided
between a positive (plus) voltage supply terminal D
of the reference voltage generating circuit F and the
external power supply source V_{CC} . In the case of the
15 circuit shown in Fig. 56, an N-channel MOS transistor
is connected between the grounded terminal of the
reference voltage generating circuit F and the ground
potential. By varying the gate voltage of the P-channel
MOS transistor T_{M200} or that of the N-channel MOS
20 transistor T_{M210} , the current value of the reference
voltage generating circuit F can be easily controlled.
In the circuit shown in Fig. 55, for example, when
the potential at the gate terminal 200 is lowered, the
resistance of the P-channel MOS transistor T_{M200} is
25 decreased, whereby the current flowing to the reference
voltage generating circuit F is increased. On the
other hand, when the potential at the gate terminal
200 is increased, the resistance of the P-channel MOS

1 transistor T_{M200} is increased, resulting in that the
current flowing to the reference voltage generating
circuit F is decreased. Thus, according to the
embodiment shown in Fig. 55, the potential at the terminal
5 200 is lowered when the semiconductor device including
the reference voltage generating circuit F is in the
operating state, while it is risen in the standby state,
whereby fluctuation in the voltage value due to noise
or the like can be prevented in the operating state
10 with the power consumption being reduced in the standby
state because of the decreased current. Also in the
case of the embodiment shown in Fig. 56, similar effects
can be attained by rising the potential at the terminal
210 in the operating state while lowering it in the
15 standby state. Since an N-channel MOS transistor is used
in the circuit shown in Fig. 56, the gate width can be
decreased greater than that of the P-channel MOS transistor
used in the circuit shown in Fig. 55. Thus, the circuit
configuration shown in Fig. 55 allows the area occupied
20 by the circuit to be decreased when compared with the
circuit shown in Fig. 55. It should further be
added in connection with the circuits shown in Figs.
55 and 56 that insertion of the MOS transistor between
the power supply source and the reference voltage
25 generating circuit involves lowering in the net voltage
applied to the reference voltage generating circuit
owing to the resistance between source and drain of
the MOS transistor. However, since the output voltage

1 V_{I1} of the circuit shown in Fig. 37 or 45 is held
substantially at a constant value independent of the
power supply voltage, as will be seen from the
expression (15), the current control can be carried out
5 without exerting any appreciable influence to the
voltage characteristic.

As the driver circuits for the address
buffer, decoder, clock driver or the like operating
with the power supply from the control line 5I' in the
10 circuit shown in Fig. 54, one of the circuits shown
in Figs. 9 to 17 may be used by replacing V_{CC} by V_I' .
If desired, the voltage V_I' may be utilized as the
control voltage in the circuits shown in Figs. 7 and
8. Although illustration of logic circuits such as
15 NAND circuit used for the decoder is omitted in Figs.
7 to 17, it will readily occur to those skilled in the
art to replace the circuit DDIV shown in Fig. 11 with
a NAND circuit, by way of example. By the way, in
applications where the load capacitance is large, high-
20 speed operation can be accomplished by using the
BiCMOS circuit. In this connection, it is to be noted
that when the breakdown strength of the bipolar
transistor Q_3 in the circuits shown in Figs. 8, 12 and
so forth is sufficiently great, the collector potential
25 may be left at the level of the external voltage V_{CC} .
In that case, since the collector current is supplied
from the external power supply V_{CC} , a major proportion
of the charging current is derived from V_{CC} , as a

1 result of which the voltage V_I' is sufficient to be
capable of supplying only the base voltage. With this
circuit arrangement, the current supply from V_I' can
be reduced while assuring the stability of the circuit
5 characteristics because the collector potential
scarcely exert influence to the circuit character-
istics so long as the collector potential lies within
the range in which the bipolar transistor is not
saturated. In this way, the voltage V_I' can be held
10 more stably. Further, it is noted that in the first
stage of the address buffer to which external signal
is directly inputted, there arises a large penetration
current when amplitude of the externally inputted
signal is inadequate. Accordingly, if V_I' is used as
15 the power supply for this stage of the address buffer,
the current supplied from the voltage source V_I' is
increased, making it difficult to maintain the voltage
 V_I' to be constant. To deal with this problem, it is
possible to operate only the first stage of the address
20 buffer with the external voltage V_{CC} .

Next, an exemplary embodiment of the
invention for controlling the charge/discharge of the
data line or wire by referring to Fig. 57.

In the DRAM, it is practically performed to
25 charge and discharge the paired data wires through a
well known sense amplifier composed of P-channel and
N-channel MOS transistor in dependence on information
read out from a memory cell (constituted by one MOS

1 transistor and one capacitor). At that time, the
quantity of electric charge Q_C stored in the capacitor
of the memory cell is determined by a product of the
data line voltage V_{DL} and the capacity C_S of the
5 capacitor. In view of the reliability of the DRAM, it
is desirable to maintain the above-mentioned charge
quantity Q_C to be stable. Accordingly, by making the
data line voltage V_{DL} independent of the external
power supply voltage V_{CC} and temperature, highly stable
10 and reliable operation insusceptible to the influence
of external conditions can be ensured. Furthermore,
by setting the data line voltage V_{DL} at a value lower
than the external power supply voltage V_{CC} within the
range in which operation is affected by no adverse
15 influence, the power consumption can be reduced. In
a modern M-bit DRAM, for example, it is necessary to
charge simultaneously 1024 pairs of data lines at a
high speed. In that case, the capacity in total of
these data lines amounts to as large a value as on the
20 order of 500 to 1000 pF, drive transistor Q_D . When
the transistor Q_2 is off (non-conduction) with Q_1 being
on, the transistor is turned off. In the mirror circuit,
the current inlet of the internal current supply is
represented by i/n , the gate width of the MOS transistor
25 is represented by w/n and the gate width of the
transistor Q_D is by W , the ON-current (current in
the conducting state) of the output drive transistor
 Q_D is a constant current i . By setting the ratio of

1 i/n to be constant, the drive current of the transistor
 Q_D can remain substantially constant even when the
factor w or gate width and the threshold value of the
transistor is changed due to deviation in the fabrication
5 process condition. The reason for selecting i/n and
 w/n for the involving the problem concerning the
transient current, which of course should preferably
be reduced. Further, in order to reduce the occurrence
of noise, accompanying the charge and discharge, it
10 is desirable to carry out symmetrically the charge and
the discharge of the data line.

According to another embodiment of the inven-
tion, it is therefore proposed to make the data line
voltage V_{DL} equal to the aforementioned voltage V_I'
15 through the control by the voltage transformer (limiter)
circuit described hereinbefore to thereby nullifying
the external voltage dependency as well as the tempera-
ture dependency and at the same time to reduce the
power consumption by lowering the voltage V_{DL} than
20 V_{CC} while reducing the transient current and noise
mentioned above by controlling the rate of charging and
discharging the data line. Now, this embodiment will
be described. Charging of the data line is performed
by the driver circuit DRV connect to a common line cl
25 of a flip-flop constituting a part of the sense amplifier
composed of a P-channel MOS transistor. The instant
embodiment is characterized in that the above-mentioned
drive circuit DRV is constituted by a current mirror

1 circuit and a comparator, wherein the current mirror
circuit is controlled by a sort of inverter constituted
by transistors Q_1 and Q_2 . When the transistor Q_2 is
turned on with the transistor Q_1 being off, the current
5 mirror circuit is formed through cooperation by a
transistor Q_3 , a constant current supply source (i/n)
and an output 2 drive transistor Q_D . When the transistor
 Q_2 is off (non-conducting) with Q_1 being on, the
transistor is turned off. In the mirror circuit, the
10 current inlet of the internal current supply is repre-
sented by i/n , the gate width of the MOS transistor is
represented by w/n and the gate width of the transistor
 Q_D is by W , the ON-current (current in the conducting
state) of the output drive transistor Q_D is a constant
15 current i . By setting the ratio of i/n to be constant,
the drive current of the transistor Q_D can remain
substantially constant even when the factor w or gate
width and the threshold value of the transistor is
changed due to deviation in the fabrication process
20 condition. The reason for selecting i/n and w/n for the
constant current supply source is for the purpose of
diminishing the current consumption as well as the
area to be occupied. It is preferred to select n to
be greater.

25 The comparator serves to compare the output
voltage V_I' (e.g. 4 volts) of the voltage transformer
(limiter) circuit and the output voltage V_O . When V_I'
is higher than V_O , the output of the comparator is a

1 voltage of high level. Reversely, when V_I' is lower
than V_O , the comparator outputs a voltage of low
level.

Now, description of operation will be entered.

5 Ordinarily, the DRAM is implemented as a so-called half-precharge type DRAM in which the paired data lines are set at a voltage value approximately equal to a half of the data line voltage V_{DL} during the precharge period. Accordingly, the common drive
10 line cl or all the paired data lines are precharged to the level of $V_{DL}/2$ during the precharge period. When a pulse is applied to a selected one of the word lines in this state, there make appearance minute differential read-out signals on each pair of the
15 data lines, as illustrated typically by D_O and $\overline{D_O}$ in Fig. 58. Subsequently, the low voltage is discharged to 0 volt with the high voltage being charged to V_I' by the sense amplifier constituted by N-channel and P-channel MOS transistors. Discharge is effectuated
20 through the MOS transistor T_{N2} . The following description will be directed only to the charging operation. The common line cl is driven by application of an input pulse ϕ . When the input pulse ϕ is ON (i.e. high voltage is inputted), the output voltage of a control
25 circuit AND assumes a high voltage level, while the gate voltage V_G of the transistor Q_D assumes the same level as the output voltage V_s of the constant current supply source, whereby the load is driven with the

1 constant current i by the drive transistor Q_D . As
a result of this, the load voltage V_O rises up at
a constant rate from the level $V_I'/2$. However, when
the load voltage V_O exceeds V_I' , the comparator
5 operates to cause the output of the control circuit AND
to assume a low level, as a result of which the
transistor Q_1 is turned on with Q_2 being off. Thus,
the drive transistor Q_D is turned off, whereby the
output voltage V_O is clamped at a level substantially
10 equal to V_I' . Consequently, one of the paired data
lines is charged approximately to V_I' from the level
 $V_I'/2$.

It will be appreciated that the discharge
rate is controlled as in the case of the charging
15 operation since the N-channel MOS transistors T_{M3} , and
 T_{N2} form a current mirror circuit in response to
application of the input pulse ϕ .

According to the embodiment described above
which allows the data line voltage V_{DL} to be approximately
20 equal to the voltage V_I' , the temperature dependency
of the data line voltage V_{DL} can be zeroed while the
dependency on the external supply voltage V_{CC} can be
nullified within a desired range. Furthermore, since
the data line can be charged with a substantially
25 constant current, the charging of the data lines can
be achieved at a high speed without being accompanied
with any appreciable increase in the transient current.
Besides, by keeping the current i_O to be constant,

1 influence of fluctuation in the source voltage and
deviation in the fabrication process conditions can
be suppressed to minimum. Additionally, the power
consumption can be reduced by virtue of the low data
5 line voltage. Finally, possibility that the data line
charging and discharging can be carried out at the same
speed is advantageously effective in noise reduction.

Now, an exemplary embodiment of the word
line drive circuit will be described. In the DRAM,
10 the voltage on the word line is set at a level higher
than that of the data line about 2 volts. By way of
example, if the data line voltage is 4 volts, that of
the line must be about 6 volts. Thus, there exists
a need for the means for rising the word line voltage
15 beyond the external supply voltage V_{CC} which is
typically 5 volts. The circuit for driving the word
line with a voltage V_H higher than the external supply
voltage V_{CC} may be realized in such configuration shown
in Fig. 59, by way of example. The circuit for
20 generating the voltage V_H will be described herein-
after.

Operation of the circuit shown in Fig. 59
will be explained by reference to a voltage waveform
diagram shown in Fig. 60. When a high potential
25 makes appearance at a terminal C in the state in which
the potential at a terminal E is high, the potential
at the line F is set at a level of $V_A - V_{T11n}$ (Fig. 60)
by an N-channel MOS transistor T_{11} . Subsequently, when

1 the potential at E becomes low, a P-channel MOS
 transistor T_{12} is turned on, resulting in that the
 potential at F is V_H . As a consequence, a P-channel
 MOS transistor t_{13} is turned off with an N-channel MOS
 5 transistor T_{14} being on, while a bipolar transistor
 T_{15} is turned on with an N-channel MOS transistor
 T_{66} being off, whereby the output W is set to zero
 volt. Parenthetically, when the potential on the line
 F rises up to V_H , the potential at terminals A and C
 10 remains zero with the transistor T_{11} being off. Accord-
 ingly, lowering of the potential at F due to the current
 flow from F to C will never take place. On the other
 hand, when the potential at the terminal C becomes
 low in the state in which the potential at the terminal
 15 E is high, the transistor T_{11} is turned on, resulting
 in that the same low potential makes appearance at both
 terminals F and C. As a result of this, the
 transistor T_{13} is turned on with the transistors T_{14}
 and T_{16} being both off, resulting in that the potential
 20 V_H makes appearance at a circuit node G, whereby
 the output D assumes rapidly a high potential level of
 $V_H - V_{BE}$ (Fig. 60). In conjunction with this circuit,
 it is noted that when the period t_{CE} (Fig. 60) intervening
 between a time point at which the terminal C assumes the
 25 high potential and a time point when the potential at
 E becomes low is long, the potential at E remains at
 the high level of $V_A - V_{T11n}$ for a time, a penetration
 current flows through the transistors T_{13} and T_{14} , as

1 a result of which there may exist a period during
which the potential at D remains at a low level.
Accordingly, it is desirable to shorten the period t_{CE} .
This can be accomplished by changing over the potential
5 at E to low level simultaneously with appearance of
high potential at C. Thus, the above-mentioned
problem can be solved.

According to the circuit described above,
the word line can be charged to the potential level
10 of $V_H - V_{BE}$ at a high speed by virtue of employment
of the bipolar transistor at the output stage. It is
however to be mentioned that the output may be directly
led out from the circuit point G without using the
bipolar transistor 15, as shown in Fig. 7A. In that
15 case, the output voltage rises up to the level V_H .
Accordingly, the voltage V_H equal to the desired word
line voltage can be generated. This means that the
design of the voltage source G can be much facilitated
when compared with the design in which the bipolar
20 transistor is used. Further, since the circuit under
consideration can be constituted by the MOS transistors,
the fabrication process is correspondingly facilitated.
It should be added that in the case of the circuit
shown in Fig. 59, a MOS transistor may be inserted in
25 succession to the power supply for the purpose of
controlling the operation speed, as described herein-
before in conjunction with the circuit shown in
Fig. 13.

1 Fig. 61 shows an exemplary embodiment of
the circuit for obtaining a high voltage not lower than
the external voltage V_{CC} on the basis of the voltage
 V_I' , and Fig. 62 is a waveform diagram for illustrating
5 operation of the above-mentioned circuit. In the
following, operation of the circuit shown in Fig. 61
will be described by reference to Fig. 62.

 The circuit shown in Fig. 61 serves for
boosting the terminal voltage V_H in synchronism with
10 a signal \overline{RAS} in the DRAM. When the DRAM starts operation
in response to the signal \overline{RAS} of a low level, a pulse
signal ϕ_{1ps} transits or shifts to a high level and
signals ϕ_{1s} and ϕ_{1SA} shifts to high levels, respectively,
as illustrated in Fig. 62. As a result, lines G1
15 and G2 of those G1, G2, G3 and G4 precharged to the
same potential as the external power supply voltage
 V_{CC} are boosted by MOS capacitances TMC_{221} and TMC_{222} ,
as a result of which currents flow to G4 and G3 from
G1 by way of MOS transistors TM_{229} and TM_{42A} , whereby
20 the potentials at the lines G3 and G4 are increased.
At this time point, since the line G2 is boosted
higher than the external voltage V_{CC} , the potentials at
G3 and G4 can be increased without being limited to the
threshold values of the MOS transistors TM_{229} and
25 TM_{22A} , respectively. Next, the signals ϕ_{1s} and ϕ_{1SA}
transit to low level with ϕ_{2s} and ϕ_{43s} shifting to
high level. Then, the potential at G1 and G2 transit
to low level while the line G3 and G4 are boosted up.

1 At that time point, the potential at G2 becomes zero
 volt since the MOS transistor TM_{22B} is turned on in
 response to the high level of ϕ_2 , whereby the MOS
 transistor TM_{22A} is turned off. Thus, the potential
 5 at G2 is prevented from being increased under the
 influence of deviation in the timing of the pulse signal
 ϕ_{2S} or due to coupling noise. Consequently, a current
 flows from G3 to the terminal 5I2 through the MOS
 transistor TM_{22C} , whereby the terminal 5I2 is boosted.
 10 Because of the presence of a serial connection of six
 diodes between the gate of the MOS transistor TM_{22C}
 and the terminal 5I1', the potential at G4 is clamped
 to the level of $V_{CL} + 6V_{BE}$. As a consequence, the
 voltage at V_H is clamped to the level of $V_I' + 6V_{BE} -$
 15 V_{T22C} , where V_{T22C} represents the threshold voltage of
 the MOS transistor TM_{22C} . When the V_I' is set at 4
 volts with V_{BE} being set at 0.8 volt while V_{T22C} is
 set at 0.8 volt, by way of example, then, the voltage
 at V_H is 8 volts. In the illustrated embodiment, six
 20 diodes are used. By changing the number of these
 diodes, it is possible to prevent the voltage V_H from
 exceeding the voltage V_I' by a predetermined value.
 Accordingly, when the word driver, for example, is
 connected to V_H , the word line voltage can be controlled
 25 to a desired value. Subsequently, when the signal \overline{RAS}
 of the DRAM assumes a high level, the signals ϕ_{2S} and
 ϕ_{3S} are reset to the low level with ϕ_{1SP} and ϕ_{2PS} being
 set to high and low levels, respectively. As a

1 result, the potential at G5 is boosted up from the
 MOS capacitance TM_{C220} , as a result of which the
 gate voltages of the MOS transistor TM_{225} , TM_{226} ,
 TM_{227} and TM_{228} are boosted higher than the external
 5 power supply voltage V_{CC} by way of the P-channel MOS
 transistor TM_{221} , whereby the potentials at G1, G2, G3
 and G4 are set to the potential level of V_{CC} through
 the above-mentioned MOS transistors to thereby restore
 the initial state. It should be mentioned that the
 10 MOS transistor TM_{223} serves to prevent the drain of
 the MOS transistor TM_{224} from being applied with a
 high voltage to thereby protect that transistor TM_{224} .
 When the series connection of diodes is employed, the
 voltage V_H is imparted with temperature dependency
 15 because the voltage V_{BE} exhibits a temperature dependency.
 For suppressing the temperature dependency of the
 voltage V_H , the amplitude of the pulse signals ϕ_{1S} to
 ϕ_{3S} may be selected equal to V_I' rather than V_{CC} with
 the clamping circuit being spared. In this case for
 20 obtaining the desired voltage value at 5I2, there
 may be employed such a circuit as shown in Fig. 63.
 By obtaining a high voltage V_{CH}' by using the circuit
 shown in Fig. 63 in the circuit of Fig. 61, a voltage
 given by $V_{REF} \times (R_{631} + R_{632})/R_{632}$ is outputted at
 25 5I2. As the reference voltage V_{REF} , there can be
 utilized the voltage V_I' or other voltage having a
 temperature dependency which can cancel out the
 temperature dependency of the voltage V_{BE} of the bipolar

1 transistor Q_{631} . As will be appreciated from the above
description, there can be obtained at 5I2 a voltage
higher than V_{CC} . As described above, V_H is boosted
up on the operating state in synchronism with the
5 signal \overline{RAS} without being accompanied with the boosting
operation in the standby state in which no current
supply from V_H is required, whereby the operation can
be realized with low power consumption. However, the
standby state may possibly continue over an extended
10 period in dependence on the operating condition. In
that case, it is conceivable that the potential V_1 at
 V_H might be lowered for some reason such as leakage.
This problem can however be solved by providing
separately a circuit for compensating for the leakage
15 in the standby state. To this end, the circuit described
above in conjunction with Figs. 61 to 63 in which,
however, the capacitance and the size of the transistors
are reduced for thereby lowering the current driving
capability may be additionally and separately provided
20 so as to be operated independent of the signal \overline{RAS} .
Alternatively, such a circuit as shown in Fig. 64 may
be provided. In the following, operation of the
circuit shown in Fig. 64 will be described by reference
to Fig. 65. When a signal $\overline{\phi_0}$ is at low level, circuit
25 points G_{240} and G_{241} as well as V_H are precharged to
a level approximating to the external voltage V_{CC}
by way of MOS transistors TM_{240} , TM_{241} and TM_{243} .
When ϕ_0 subsequently rises up to a high level, the

1 outputs of inverters I_{241} and I_{242} assume high and low
 levels, respectively. As a result, G_{240} is boosted
 up beyond V_{CC} , whereby a current flows to G_{240} to
 increase the potential thereat. When ϕ_0 becomes
 5 low, the outputs of the inverters I_{241} and I_{242} assume
 low and high levels, respectively, resulting in that
 G_{241} is further boosted up to cause a current to flow
 toward V_H . In this way, by lowering and rising the
 level of the signal ϕ_0 periodically, the potential
 10 at V_H is increased. As the potential at V_H is risen,
 the potential V_{G246} at G_{246} becomes high in accordance
 with the relation of $V_H - 6V_{BE}$ by way of the diodes
 QD_{240} to QD_{245} . When the voltage value given by $V_I' -$
 $V_{T246} + 6V_{BE}$ is exceeded by the potential at V_h upon
 15 setting of the threshold value of the MOS transistor
 TM_{246} at $-V_{T246}$, then $V_{G246} = V_I' - V_{T56}$, whereby the
 MOS transistor TM_{246} is turned off, resulting in that
 the potential D_{247} is set to zero by the MOS transistor
 TM_{247} . As a consequence, the voltage at the output
 20 O_5 of a NAND circuit NA_{240} is fixed at a high level,
 to thereby stop the voltage boosting operation. There-
 after, when the potential at V_H is lowered by the current
 I_h flowing out from the control line 5I2 below the
 level given by $V_I' - V_{T246} + 6V_{BE}$, then the MOS
 25 transistor TM_{246} is again turned on to restart the
 V_H boosting operation. In this way, the potential at
 V_H can be maintained at a level of $V_I' - V_{T246} + 6V_{BE}$
 which is higher than the external power supply voltage

1 V_{CC} according to the embodiment shown in Fig. 64.
 By way of example, when V_I' is set at 4 volts, V_{T246}
 is at 0.5 volt and V_{BE} is at 0.8 volt, then V_H is at
 the potential of 8.3 volts. In this manner, according
 5 to the instant embodiment which corresponds to a
 combination of the charge pump circuit and the level
 shift circuit described hereinbefore, the output voltage
 V_H can be maintained at a constant voltage higher than
 the external power supply voltage V_{CC} . Needless to
 10 say, the number of the clamping diodes QD_{240} to QD_{245}
 may be increased or decreased, as occasion requires.
 Further, in case the current flowing through the
 diodes QD_{240} to QD_{245} from V_H is excessively large, the
 diode QD_{245} may preferably be replaced by a bipolar
 15 transistor Q_{245}' , wherein the collector thereof is
 connected to V_{CC} with the base being connected to
 the output terminal of the diode QD_{244} , as is shown in
 Fig. 66. With this circuit configuration, the above-
 mentioned current can be decreased to $1/h_{FE}$. The
 20 number of the diodes QD can be determined so that
 difference between the voltages V_H and V_H' is equal to
 a desired value. Further, the MOS transistor TM_{248}
 may be replaced by other element such as a resistor.
 In case the MOS transistor is employed, high resistance
 25 value can be realized with a relatively small area for
 occupation by selecting larger the gate length L_g
 when compared with the gate width. In the illustrated
 embodiment, it is assumed that the pn-junction type

1 diodes are employed. In this connection, it will be
 readily understood that such pn-junction type diode can
 be realized, for example, by connecting together the
 base and collector of the bipolar transistor. In that
 5 case, the diodes can be formed simultaneously with the
 bipolar transistors, which in turn means that the
 fabrication process can be correspondingly simplified.
 Such simplification can further be promoted by
 realizing the resistor by using the base layer of the
 10 bipolar transistor. Since the forward bias voltage V_{BE}
 of the pn-junction type diode is ordinarily about 0.8
 volt, the difference between the voltages V_H and V_I' in
 the device shown in Fig. 64 can assume only a value
 that is based on the unity voltage of 0.8 volt. There
 15 may however arise such a case where it is required
 that difference between the voltage V_h and V_I' be set
 at other value than $0.8n$ volts ($n = 1, 2, \dots$). In
 that case, a Schottky diode having the forward voltage
 V_F on the order of 0.4 volt may be used. Then,

$$V_H = V_I' - V_{T246} + iV_F$$

20 Thus, the value V_H can be set on the basis of the unit
 voltage of 0.4 volt. Of course, a N-channel MOS diode
 may be used, as is shown in Fig. 67. In this case,

$$V_H = V_I' - V_{T246} + iV_{TMA}$$

1 where V_{TMA} represents the N-channel MOS diode T_{MA} .
 Thus, the potential difference of concern can be varied
 on the basis of the unity voltage of V_{TMA} . A circuit
 shown in Fig. 68 may be used in place of diode for
 5 producing the desired potential difference. Referring
 to Fig. 68, the potential difference making appearance
 across the terminals 3A and 3B is given by

$$V_{BE}(1 + R_A/R_B)$$

Thus, the potential difference can be varied continuously
 by varying the resistance ratio of R_A/R_B . Other versions
 10 and modifications are possible within the purview of
 the present invention. Fig. 69 shows a version of
 the level shift circuit shown in Fig. 64. It will be
 seen that the level shift circuit shown in Fig. 69 is
 constituted by using only N-channel MOS elements. More
 15 specifically, the clamping diodes are realized as the
 N-channel MOS diodes, and the bipolar transistor Q_1
 and the resistor R are replaced by N-channel MOS
 transistors TM_{51} and TM_{52} , respectively. According to
 the embodiment shown in Fig. 69, the relation between
 20 V_H and V_I' is given by

$$V_H = V_I' - V_{T246} + V_{TM51} + nV_{TD}$$

where V_{TM51} represents the threshold voltage of the
 transistor TM_{51} and V_{TD} represents the threshold voltage

1 of the MOS diode. It is apparent that the potential
difference can be established on the basis of the
unity voltage of V_{TD} . In the case of this embodiment,
the current flowing through the N-channel MOS diodes
5 T_{MD51} to T_{MD5i} is only the bias current I_N flowing
through the N-channel MOS transistor T_{M53} . Accordingly,
it is unnecessary to increase the current supply
capacity of 5I2 beyond the requisite value. Further,
since the circuit shown in Fig. 69 can be constituted
10 only by the MOS transistors without need for the use of
bipolar transistor, this embodiment is suited advan-
tageously for application to LSI which is composed
only of MOS transistors. The gate voltages, gate
lengths and the gate widths of the MOS transistors T_{M51}
15 and T_{M53} may be so determined that the currents I_R and
 I_N can assume desired values, respectively. By way
of example, by setting the current I_R at a value ten
times as high as that of the current I_L , fluctuation
in the drain current of the MOS transistor T_{M51} can
20 be suppressed to about 10%, whereby V_L can be maintained
to be substantially constant. In case a problem arises
in connection with the temperature characteristics of
the clamping circuit in the embodiment described
above, the voltage supplied to the MOS transistor T_{M246}
25 may be imparted with such temperature dependency which
can compensate for that of the clamping circuit.

The present invention can be effectively and
advantageously applied to SRAMs in addition to the DRAMs.

1 Fig. 70 shows an exemplary embodiment of the SRAM in
which the memory cell is constituted by using a N-
channel MOS transistor and a resistor. High stable
and reliable operation of the SRAM can be accomplished
5 by performing the control on the drive circuit and
the differential amplifier constituting the peripheral
circuitry of the SRAM in the manner described herein-
before. Besides, by supplying the voltage applied to
load resistors R_{C1} and R_{C2} of the memory cell from the
10 voltage transformer circuit according to the invention
instead of the external power supply V_{CC} , the
temperature dependency as well as the external voltage
dependency of the characteristics of the memory cell
can be eliminated, whereby the soft-error withstanding
15 capability can be enhanced. Thus, the extremely stable
memory operation can be realized. Further, since the
current supplied through R_{C1} and R_{C2} , i.e. the memory
cell hold current, is an extremely small DC current
which is substantially constant, it is possible to
20 maintain the voltage to be constant with high accuracy.
Besides, the reliability can further be improved by
controlling the data line voltages DL and \overline{DL} (i.e.
the write voltages) as well as the word line (W)
voltage to be stable. To this end, the write voltage
25 can be determined on the basis of the voltage V_I
derived according to the invention as described herein-
before, whereby the temperature dependency as well as
the external-voltage dependency can be essentially

1 nullified with the reliability being further enhanced.

Moreover, the present invention can be applied to other logic LSIs than the memory. In the control circuit shown in Fig. 53, the characteristics of the peripheral circuit is detected at 6. It should however be understood that the detection may be carried out at other various circuit points in dependence on the intended purposes. By way of example, duration required for amplification of the feeble (weak) signal by the sense amplifier may be detected, wherein the result of the detection may be utilized for changing the driving voltage and the driving current of the sense amplifier to thereby control the operation characteristics of the memory cell array. Of course, other control methods may occur to those skilled in the art. Although the invention has been described on the assumption that the MOS transistor and/or bipolar transistor are employed as main constituent elements, it will be appreciated that the principle of this invention can be equally applied without any substantial modification to the circuits constituted by compound semiconductor elements such as GaAs-elements. As the variable factors of the characteristics, element constants of MOS transistor are mainly considered. However, it goes without saying that variations in the current amplification factor, cut-off frequency and the forward bias voltage of the bipolar transistor can be similarly taken into consideration. Further, although the foregoing description of

1 the embodiments has been made primarily with the
intention to maintain the various characteristics to be
constant. However, when such deviation in the
fabrication process condition as the variations in the
5 gate length and the threshold voltage as well as changes
in the operating condition such as changes in the
temperature and the power supply voltage have tendency
to contribute to the increasing in the operation speed
of the semiconductor, control may be made such that the
10 operation speed is further increased, by applying
correspondingly the teaching of the present invention.
Reversely, when the deviation in the fabrication
process condition and variation in the operating
condition tend to lower the operation speed of the
15 semiconductor device, control may be made such that the
operating speed is further decreased.

Although the foregoing description has been
mainly directed to the utilization of TTL interface,
it is self-explanatory that the invention can equally
20 be carried out with other type of interface such as
ECL.

As will now be appreciated from the foregoing
description, there can be realized semiconductor
devices enjoying high stability and reliability regard-
25 less of deviations and variations in the fabrication
process condition and the operating condition according
to the present invention. Besides, since high yield
can be assured even in the fabrication on the mass-

1 production basis, the semiconductor devices can be
manufactured inexpensively when compared with the
hitherto known devices.

It is further understood by those skilled
5 in the art that the foregoing description is a preferred
embodiment of the disclosed device and that various
changes and modifications may be made in the invention
without departing from the spirit and scope thereof.